A 320 Gb/s-Throughput Capable 2×2 Silicon-Plasmonic Router Architecture for Optical Interconnects

Sotirios Papaioannou, K. Vyrsokinos, O. Tsilipakos, A. Pitilakis, K. Hassan, J.-C. Weeber, L. Markey, A. Dereux, S. I. Bozhevolnyi, A. Miliou, E. E. Kriezis, and N. Pleros

***Abstract*—We demonstrate a 2×2 silicon-plasmonic router architecture with 320 Gb/s throughput capabilities for optical interconnect applications. The proposed router platform relies on a novel dual-ring Dielectric-Loaded Surface Plasmon Polariton (DLSPP) 2×2 switch heterointegrated on a Silicon-on-Insulator (SOI) photonic motherboard that is responsible for traffic multiplexing and header processing functionalities. We present experimental results of a Poly-methyl-methacrylate (PMMA)-loaded dual-resonator DLSPP waveguide structure that uses two racetrack resonators of 5.5 μm radius and 4 μm-long straight sections and operates as a passive add/drop filtering element. We derive its frequency-domain transfer function, confirm its add/drop experimental spectral response, and proceed to a circuit-level model for dual-ring DLSPP designs supporting 2×2 thermo-optic switch operation. The validity of our circuit-level modeled 2×2 thermo-optic switch is verified by means of respective full vectorial three-dimensional Finite Element Method (3D-FEM) simulations. The router setup is completed by means of two 4×1 SOI multiplexing circuits, each one employing four cascaded second order micro-ring configurations with 100 GHz spaced resonances. Successful interconnection between the DLSPP switching matrix and the SOI circuitry is performed through a butt-coupling design that, as shown via 3D-FEM analysis, allows for small coupling losses of as low as 2.6 dB. The final router architecture is evaluated through a co-operative simulation environment, demonstrating successful 2×2 routing for two incoming 4-wavelength Non-Return-to-Zero (NRZ) optical packet streams with 40 Gb/s line-rates.**

***Index Terms*—Dielectric-loaded surface plasmon polariton waveguide, optical interconnects, optical routing, racetrack/ring resonator, silicon-on-insulator, silicon multiplexer, thermo-optic switching.**

Manuscript received March 29, 2011; revised June 17, 2011; accepted August 30, 2011. Date of publication September 08, 2011; date of current version October 19, 2011. This work was supported by the EC FP7-ICT Project PLATON under Contract 249135.

S. Papaioannou, A. Miliou, and N. Pleros are with the Department of Informatics, Aristotle University of Thessaloniki, Thessaloniki, Greece (e-mail: sopa@csd.auth.gr).

K. Vyrsokinos is with the Informatics and Telematics Institute, Center for Research and Technology Hellas, Thessaloniki, Greece.

O. Tsilipakos, A. Pitilakis, and E.E. Kriezis are with the Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, Thessaloniki, Greece.

K. Hassan, J.-C. Weeber, L. Markey, and A. Dereux are with the Laboratoire Interdisciplinaire Carnot de Bourgogne (ICB), UMR 5209 CNRS-Université de Bourgogne, F-21078 Dijon Cedex, France.

S. I. Bozhevolnyi is with the Institute of Sensors, Signals and Electrotechnics, University of Southern Denmark, Odense, Denmark.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JLT.2011.2167315

I. Introduction

With parallel processing being the accepted methodology for boosting High Performance Computing (HPC) performance improvements, multiple processing cores are required to exchange a vast amount of information that cannot be sustained by bandwidth-limited electrical interconnects [1]. Limitations in bandwidth and excessive energy as well as footprint requirements arising from electrical wiring have led to a clearly shaped roadmap for bringing optics "into-the-box", designating the shift towards optical interconnect solutions as the most promising paradigm for accessing Exascale processing powers [2], [3]. In this perspective, silicon photonics appears as the dominant technology platform for the realization of low-loss, chip-scale and CMOS-compatible optical interconnects [4], [5]. Silicon-on-Insulator (SOI) technologies have proven capable of hosting most of the critical functions required for optical interconnect applications [6], leading to remarkable achievements both with respect to chip-level transceiver [7], [8] and routing [9] circuitry applications. This progress has, in turn, spurred intense research towards next-generation Chip Multi-Processor (CMP) architectures relying on optical interconnect planes, clearly indicating the important size and energy savings when properly adapting the architectural CMP framework to the operational requirements of photonics [10]–[13].

However, with chip size reduction and energy savings being the driving forces in next-generation optical interconnect technology, the emerging research discipline of plasmonics appears as a promising candidate for challenging the stronghold of silicon. Plasmonics relies on the propagation of electromagnetic waves known as Surface Plasmon Polaritons (SPPs) along a metal-dielectric interface, and is expected to access processing characteristics that lie beyond the reach of photonics and electronics [14], [15]. Strong mode confinement available with SPP waves allows for the deployment of photonic circuits with subwavelength dimensions, breaking thereby the size barriers of traditional diffraction-limited optics [16]. Moreover, the presence of metal-dielectric interfaces amidst SPP-based circuitry allows for a seamless interface between electrical and optical signals, providing in this way a natural energy-efficient platform for merging broadband optical links with intelligent electronic processing.

The low-power functional portfolio of plasmonics is especially pronounced in the case of Dielectric-Loaded SPP (DLSPP) waveguides that rely on the use of dielectric loading atop of metal (gold) films [17], [18]. DLSPP structures can, in

principle, be designed for different functionalities by simply selecting the proper dielectric material. Significant progress has been reported in this direction during the last years, demonstrating a whole new class of passive DLSPP circuits [19]–[21] and the first important experimental and theoretical steps towards controlling plasmon propagation via the thermo-optic effect and realizing respective switching modules [22]–[25]. Their potential for reaching system-level applications has further been strengthened by the demonstration of their successful interconnection to different waveguide platforms, including optical fibers [26] and SOI waveguides [27], and by their recent utilization for power monitoring purposes [28].

However, the development of strategy for bringing DLSPP structures into practical system-level applications at chip-scale environments is still in its infant years, the main limiting factor certainly being their high propagation losses. Similar to most plasmonic structures, DLSPP waveguides restrict signal propagation over a few tens of micrometers due to radiation absorption in metal (ohmic loss) [18]. One approach of dealing with plasmonic losses could be by using Long-Range SPP (LRSPP) waveguides [29], [30] that have also been shown to serve as the transmission platform in 4×2.5 Gb/s interconnects [29]. This roadmap comes, however, at the expense of substantially increased plasmonic-circuitry footprints, since LRSPP waveguides require mm-large bend radii (due to their weak lateral confinement), that negates the circuit size advantages expected by the employment of plasmonic technology.

In this article, we demonstrate for the first time to our knowledge a system-level application perspective of DLSPP switching structures that can optimally exploit the circuit size and low-energy advantages of the DLSPP waveguide platform. We present a 2×2 silicon-plasmonic router architecture that can provide up to 320 Gb/s throughput capabilities, using a novel dual-ring 2×2 DLSPP thermo-optic switch residing on a SOI photonic motherboard. The SOI motherboard is responsible for signal multiplexing and header processing operations, so that the high-loss but highly functional DLSPP elements are employed only where switching functionality is required, whereas all necessary passive photonic circuitry relies on low-loss SOI waveguides. The dual-resonator DLSPP configuration is experimentally characterized as an add/drop filtering element employing two racetrack resonators of 5.5 μm radius and 4 μm-long straight sections and the experimental results are verified through circuit-level analytical expressions for its frequency-domain transfer function. We extend our circuit-level model towards designing a 2×2 thermo-optic dual-ring DLSPP switch and respective results are found to be in close agreement with rigorous full vectorial 3D-FEM simulations. The router setup is completed by two 4×1 SOI multiplexing circuits (SOI-MUX) that are designed to support multiplexing of four wavelength channels spaced at 100 GHz and carrying 40 Gb/s Non-Return-to-Zero (NRZ) packet traffic each. Interconnection between the silicon and plasmonic modules is achieved by a butt-coupling technique numerically investigated through 3D-FEM simulations and shown to yield small coupling losses as low as 2.6 dB for the case of rib SOI waveguides. The final router platform is evaluated through a co-operative simulation platform incorporating the DLSPP and SOI-MUX circuit-level models into the VPI photonic network tool, showing successful 2×2 routing of two incoming 4-channel optical streams.

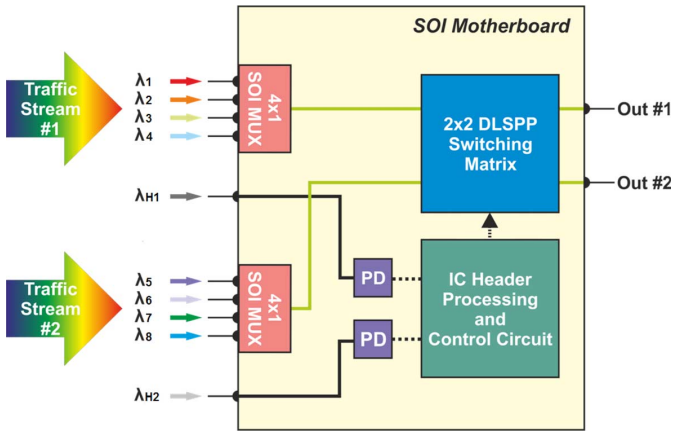

Fig. 1. Layout of the 2×2 silicon-plasmonic router architecture.

The rest of the paper is organized as follows: Section II describes the silicon-plasmonic router architecture, while Section III reports on the analysis of the dual-resonator DLSPP configuration. Sections IV and V present the 4×1 SOI-MUX layout and the silicon-plasmonic coupling approach, respectively. Finally, Section VI demonstrates simulation results for the complete 2×2 router architecture.

II. The Silicon-Plasmonic Router Architecture

Fig. 1 illustrates the block diagram of the proposed 2×2 silicon-plasmonic router platform. It employs two incoming optical streams, each one comprising four time-overlapping data wavelengths modulated with 40 Gb/s NRZ packet traffic, so that every input port supports an aggregate traffic of 160 Gb/s. A discrete wavelength is responsible for carrying the header pulse information for every incoming stream, specifying the required router output port. This multi-wavelength traffic format has been already shown to enable high throughput in SOI routing interconnects, allowing for packet-rate headers that can be easily processed by low-speed electronic control circuitry [9]. The router architecture relies on a SOI motherboard for ensuring low-loss optical interconnectivity between the router subsystems, while serving as the hosting platform for all heterogeneous technologies, including the 4×1 SOI multiplexers, the 2×2 DLSPP switching matrix, the photodiodes (PDs) and the Integrated Circuit (IC) control electronics.

The four data channels forming an incoming traffic stream are inserted through the respective router input ports and are multiplexed in a 4×1 SOI multiplexer. This multiplexed multi-wavelength data sequence will then follow the same route through the entire platform. The header section carrying the information about the router outgoing port is modulated on a separate wavelength channel that enters the router through a distinct input port. The header channel is then opto-electronically (O/E) converted in a low-speed PD conversion module that provides the respective electrical header pulses at its output. This

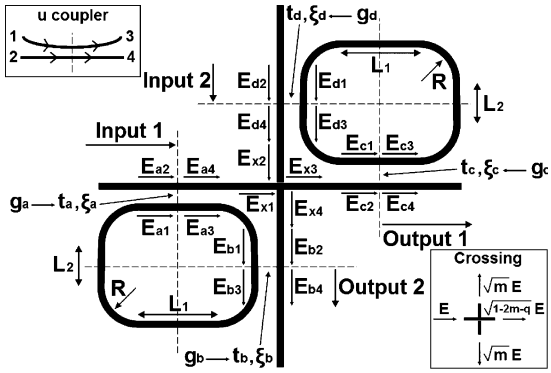

Fig. 2. Dual-resonator DLSPP-based filter layout.

electrical signal is launched as input in the IC electronic control circuit that is responsible for header processing and control signal generation. The IC circuit has two input ports for receiving the addresses of both incoming optical streams and generates the appropriate electronic control signal for driving the 2×2 DLSPP switching module. The DLSPP-based switching matrix is the router's core element, associating the incoming optical streams with the specified output ports; traffic streams #1 and #2 exit the router through the output ports #1 and #2, respectively, when the DLSPP matrix operates in its BAR state, whereas they exchange output ports when CROSS state operation of the DLSPP matrix is selected. BAR or CROSS state operation of the DLSPP unit is dictated by the electrical control signal provided by the IC.

The SOI waveguide technology relies on a rib design with 400 nm width, 340 nm height and a silicon slab layer of 50 nm thickness in order to allow for the propagation of the Transverse Magnetic (TM) optical mode supported by the DLSPP structures. As no buffering modules are employed in the router platform, contention resolution relies on deflection-based strategies adopting a prioritization scheme for the incoming optical traffic streams. The higher priority packet will leave the router through the desired outgoing port, while the lower priority stream will be directed to the second output port following an alternate route until its final destination [31].

III. The Dual-Resonator DLSPP Switch

Fig. 2 depicts the layout of a dual-resonator DLSPP configuration that serves as the thermo-optic switching element. It comprises two perpendicularly intersecting DLSPP waveguides along with two diagonally positioned DLSPP racetrack resonators. A similar architectural design has been utilized using SOI waveguide technology for switching of multi-wavelength incoming traffic [9]. However, the SOI-based layout employs large ring radii in the range of tens of micrometers aiming at generating a discrete resonant peak per inserted wavelength. This approach cannot be adopted in the case of a DLSPP-based implementation due to the high propagation losses of DLSPP structures. To this end, broadband multi-wavelength operation of the respective 2×2 dual-ring DLSPP configuration dictates that all inserted wavelengths have to reside within the passband of a single resonance. This can be ensured using small ring radii values that additionally allows for low loss device functionality.

A. Frequency Domain Transfer Function

In the following, the frequency domain transfer function of this device when acting as a passive filtering element is analytically derived for both output ports 1 and 2, assuming an incoming electrical field E_{in1} inserted through input port 1. The two racetrack resonators are considered to be identical employing two straight waveguide regions of lengths L_1 and L_2 and a curved section of radius R. The resonators are separated by the bus waveguides by gaps of size g_u, with u representing the couplers a, b, c or d shown in Fig. 2. Couplers a and c are associated with the straight sections of length L_1, while couplings at b and d are associated with the waveguide sections L_2. By denoting as E_{u1} and E_{u2} the two electrical fields arriving at the coupler u and as E_{u3} and E_{u4} the electrical fields leaving the coupler, the following relationships are valid at each coupling region:

$$E_{u3} = t_u E_{u1} + j\xi_u E_{u2} \tag{1}$$

$$E_{u4} = t_u E_{u2} + j\xi_u E_{u1} \tag{2}$$

with t_u and ξ_u representing the field transmission and coupling coefficients, respectively, satisfying the relation $\xi_u = \sqrt{1 - t_u^2}$ in the absence of coupling losses.

The 90° crossing between the two intersected waveguides is considered to introduce a power crosstalk level equal to m, so as to take into account also realistic crossing implementations where no tapering treatment of the crossing region is used [25], [32]. Denoting as E_{x1} and E_{x2} the crosspoint input signals and as E_{x3} and E_{x4} the respective output signals, field propagation at the crosspoint is governed by the following set of equations:

$$E_{x3} = \sqrt{1 - 2m - q}E_{x1} + \sqrt{m}e^{-j\varphi_m}E_{x2} \tag{3}$$

$$E_{x4} = \sqrt{1 - 2m - q}E_{x2} + \sqrt{m}e^{-j\varphi_m}E_{x1} \tag{4}$$

with φ_m standing for the additional phase acquired by the crosstalk and q denoting any additional insertion losses owing to scattering and back reflection [25].

The mathematical framework required for the transfer function extraction is completed by taking into account also the corresponding field propagation equations between all possible successive coupling regions or waveguide-crossing transitions. The propagation of an electrical field from a starting location k to an end point l can be generally expressed through multiplication with a path coefficient A_k^l, so that $E_l = A_k^l E_k = \sqrt{e^{-\alpha L}}e^{-j\varphi}E_k$, with L being the waveguide distance, α the power loss coefficient, and $\varphi = (2\pi/\lambda)n_{\text{eff}}L$ the phase acquired during propagation, where λ stands for the wavelength and n_{eff} for the effective refractive index.

Applying (1) and (2) to all employed coupling stages, using (3) and (4) and exploiting the above set of elementary propagation relationships for all possible routes in the dual-resonator layout, the transfer function can be derived by means of algebraic The electrical field transfer functions for output ports 1 and 2, respectively, are given in

$$\frac{E_{\text{op1}}}{E_{\text{in1}}} = \frac{\sqrt{1-2m-q}A_{a4}^{x1}A_{x3}^{c2}\left(t_c - t_d A_{d3}^{c1}A_{c3}^{d1}\right)\left(t_a - t_b A_{a3}^{b1}A_{b3}^{a1}\right)}{F} \tag{5}$$

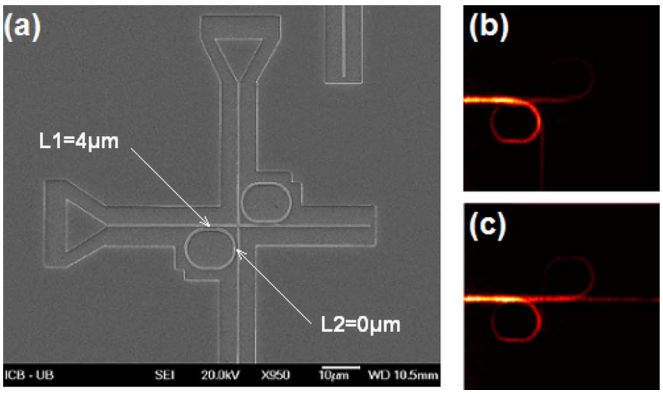

Fig. 3. (a) SEM image of the dual-resonator DLSPP add/drop filtering element. (b), (c) RLM images when light is guided to the Drop and Through port, respectively.

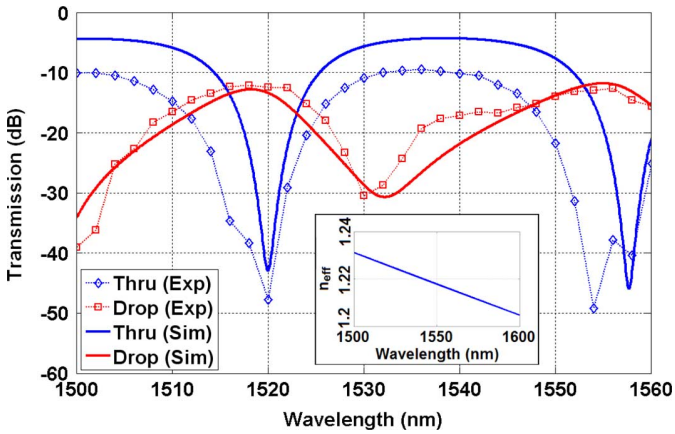

Fig. 4. Transmission spectra at Through and Drop ports of the dual-resonator DLSPP add/drop filter obtained by circuit-level modeling (solid lines) and experiment (dotted lines with markers). Inset depicts the effective refractive index for a straight DLSPP waveguide according to FEM eigenmode analysis.

and (6), shown at the bottom of the page, where the input and output electrical fields $E_{\text{in1}}, E_{\text{op1}}$ and E_{op2} are E_{a2}, E_{c4} and E_{b4}, respectively, where F is given by (7), shown at the bottom of the page.

B. Experimental and Theoretical Analysis of a Dual-Resonator DLSPP Add/Drop Filtering Element

A dual-resonator DLSPP structure performing add/drop filtering has been fabricated by a process relying on electron-beam lithography (EBL). A glass substrate is cleaned and coated with a gold thin film with a thickness of 60 nm. This thickness value prohibits strong radiation of the plasmonic mode within the substrate, allowing, however, for the detection of the mode by means of a sensitive Infra-Red (IR) Charge-Coupled Device (CCD) camera. The metal coated substrate is next spin-coated with a Poly-methyl-methacrylate (PMMA) resist at a nominal thickness of 560–580 nm. The PMMA-coated substrate is then exposed to the electron beam and the exposed areas are subsequently dissolved. Fig. 3(a) depicts the Scanning Electron Microscope (SEM) image of the fabricated dual-resonator DLSPP add/drop filtering element. Both racetrack resonators have a radius of $R = 5.5\ \mu$m and straight waveguide region lengths of $L_1 = 4\ \mu$m and $L_2 = 0\ \mu$m. The gaps g_a, g_b, g_c, g_d between the racetrack designs and the respective intersected waveguide sections are 333 nm, 328 nm, 305 nm and 384 nm, respectively.

Optical characterization has been performed by Radiation Leakage Microscopy (RLM). Plasmonic mode excitation is achieved by focusing the incident laser on one end of the input waveguides. The excited plasmonic mode radiates a fraction of its energy within the dielectric substrate at an angle corresponding to a numerical aperture of typically 1.2 to 1.3. The image is recorded by an IR CCD camera with high sensitivity through an oil immersion objective [24].

Figs. 3(b)–(c) illustrate the RLM images obtained at operating wavelengths 1520 nm and 1536 nm, respectively. The 1520 nm wave is exiting the device through its Drop-port, while the optical power at 1536 nm emerges at the Through-port. The complete experimental transmission spectra obtained for both the Through and Drop ports of the DLSPP module over the entire 1500–1560 nm spectral window are shown by the dotted lines in Fig. 4. A clear resonant behavior can be observed with the Free Spectral Range (FSR) of the Through-port resonances being equal to 36 nm. The resonant dips at the Through-port have an Extinction Ratio (ER) of more than 35 dB, while the corresponding ER value for the Drop-port resonant peaks is close to 18 dB. Insertion losses (IL) for the Through and Drop ports are -10 dB and -12 dB, respectively. The broadband characteristics of the Through and Drop port resonances can be also clearly

$$\frac{E_{\text{op2}}}{E_{\text{in1}}} = \frac{A_{x4}^{b2}A_{a4}^{x1}\left(t_b - t_a A_{a3}^{b1}A_{b3}^{a1}\right)\left(t_a - t_b A_{a3}^{b1}A_{b3}^{a1}\right)\left[\sqrt{m}e^{-j\varphi_m}\left(1 - t_c t_d A_{d3}^{c1}A_{c3}^{d1}\right) + \left(me^{-j2\varphi_m} + 2m + q - 1\right)\xi_c\xi_d A_{x3}^{c2}A_{d4}^{x2}A_{c3}^{d1}\right] - F\xi_a\xi_b A_{a3}^{b1}}{\left(1 - t_a t_b A_{a3}^{b1}A_{b3}^{a1}\right)F} \tag{6}$$

$$\begin{aligned} F = {} & \left(1 - t_c t_d A_{d3}^{c1}A_{c3}^{d1} + \sqrt{m}\xi_c\xi_d A_{x3}^{c2}A_{d4}^{x2}A_{c3}^{d1}e^{-j\varphi_m}\right)\left(1 - t_a t_b A_{a3}^{b1}A_{b3}^{a1} + \sqrt{m}\xi_a\xi_b A_{b3}^{a1}A_{a4}^{x1}A_{x4}^{b2}e^{-j\varphi_m}\right) \\ & - (1 - 2m - q)\xi_a\xi_b\xi_c\xi_d A_{b3}^{a1}A_{c3}^{d1}A_{x4}^{b2}A_{d4}^{x2}A_{x3}^{c2}A_{a4}^{x1} \end{aligned} \tag{7}$$

identified: the Drop resonance at 1520 nm has a -3 dB bandwidth close to 12 nm, while the resonant dip of the Through port at the same wavelength ensures signal suppression by more than 12 dB within a spectral band of 10 nm. These values confirm the potential of dual-resonator DLSPP structures to perform as multi-wavelength add/drop filtering elements, indicating at the same time their multi-wavelength properties when used in thermo-optic switching arrangements. The quality factor of the fabricated DLSPP-based resonator was calculated to be $\sim$77 for the Through and $\sim$115 for the Drop port at 1520 nm resonance and the propagation loss factor of the DLSPP waveguide was measured to be 0.1 dB/μm at 1550 nm.

The experimental transmission spectra of the dual-resonator DLSPP add/drop filtering module have been successfully reproduced by means of circuit-level modeling exploiting the frequency-domain transfer function of the device provided by (5) and (6). The theoretically extracted Through and Drop port transmission curves are shown by the solid lines in Fig. 4. Coupling coefficients of $\xi_a^2 = 0.6, \xi_b^2 = 0.05$, $\xi_c^2 = 0.62$ and $\xi_d^2 = 0.01$ have been used for the four coupling regions corresponding to the respective g_a, g_b, g_c, g_d gaps between racetrack and straight waveguides. The high values used for ξ_a^2 and ξ_c^2 coupling coefficients indeed correspond to the increased coupling owed to the 4 μm-long sections, while the low-level coupling induced by the $L_2 = 0$ μm sections is effectively associated with the small ξ_b^2 and ξ_d^2 coupling coefficients. A crosstalk level m and a total insertion loss factor $2m + q$ of -15 dB and -0.5 dB respectively have been considered at the crosspoint between the two intersected waveguides, with the respective phase shift φ_m equaling $\pi/2$, as predicted by 3D-FEM analysis [25].

The inset in Fig. 4 illustrates the effective refractive index n_{eff} versus wavelength curve that has been obtained by a FEM eigenmode solver for the case of a straight PMMA-loaded SPP waveguide of 500×600 nm^2 cross-section, taking into account the material dispersion of gold [33]. However, a negative offset of 0.15 has been applied to this curve before being employed in the circuit-level model. The lower n_{eff} values required for optimal fitting between theory and experiment are probably due to contributions by the racetrack bending and coupling sections that have different mode propagation characteristics compared to straight DLSPP waveguides.

The agreement between theory and experiment can be confirmed with respect to all relevant parameters, including FSR, ER and resonant bandwidth characteristics. The slight irregularity in the Drop-port resonant shapes is also efficiently predicted by theory. The irregularities at the Drop-port resonant peak shapes are the result of multiple wave interference taking place at this port, since optical crosstalk terms and optical waves originating after circulations in both racetrack structures are forced to interfere. Although the same phenomenon occurs at the Through-port, the Through-port field component emerging without any recirculating experience is much stronger in power than the respective recirculating field constituents. Therefore, the final Through-port output signal is almost insensitive to this multi-wave interference, being in good agreement with respective 3D-FEM-based theoretical findings [25]. As such, circuit-level analysis can provide reliable response predictions using simple n_{eff} calculations derived by FEM eigenmode analysis for straight DLSPP waveguides instead of solving the entire electromagnetic problem for the complicated structure of dual-resonator DLSPP design. The deviations observed between circuit-level simulations and experiment at Through-port's IL value owe presumably to measurement inaccuracies arising by the integration method employed for the optical power calculation in the RLM characterization process [24].

C. Dual-Ring DLSPP as a 2 × 2 Thermo-Optic Switch

The passive dual-resonator DLSPP structure performing as an add/drop filter can be transformed into an active switching element through the utilization of the thermo-optic effect [22]. DLSPP waveguides provide a natural interface for electrically addressing their operation exploiting thermo-optics by simply injecting an electrical current to the finite-width metallic stripe [22], [23], [25]. This yields a local temperature change in the polymer loading that can be efficiently translated in resonance tuning and, subsequently, in a change in the device's switching state. This technique enables the effective exploitation of the field enhancement at the metal-polymer interface towards requiring reduced power consumption. The thermo-optic effect has been employed in the implementation of various dynamic components based on the stripe SPP waveguide [34], [35] and has been also more recently utilized for the control of DLSPP waveguide ring resonator and Mach–Zehnder interferometric devices [23], [24]. A detailed theoretical investigation through 3D-FEM simulations of thermo-optically tunable DLSPP all-pass filters, including their temporal switching response, is presented in [22].

Following the good agreement obtained between experiment and circuit-level modeling in dual-resonator DLSPP designs acting as passive add/drop filtering modules, the circuit-level model can be used for reliable predictions of the dual-ring DLSPP's thermo-optic switching behavior by utilizing the n_{eff} values calculated for both an unheated and heated DLSPP waveguide. The optimized operation of the dual-ring DLSPP structure as a 2 × 2 switch requires, however, a slightly different design compared to the layout shown in Fig. 2. Operation as a 2 × 2 switch implies a similar performance for both input ports, indicating specific symmetry conditions in the design. This symmetry can be obtained only by having identical coupling stages (t_a, ξ_a) and (t_d, ξ_d) and, subsequently, identical values for the coupling sections (t_b, ξ_b) and (t_c, ξ_c). This means that in the case of the layout shown in Fig. 2, coupling stages a and d should be associated with the same straight waveguide length L_1 of the respective racetrack resonator and with identical gap values, so that also the remaining b and c coupling stages will be associated with the L_2 racetrack regions and, again, identical gap values.

As no experimental data have been so far reported on dual-ring DLSPP switching, the performance of the circuit-level modeled dual-ring DLSPP design when operating as a 2 × 2 thermo-optic switch has been evaluated in comparison with respective findings when 3D-FEM calculations are employed [25]. The 2 × 2 switch layout adopted in the 3D-FEM approach and used also in the circuit-level analysis is shown in Fig. 5(a), using a ring radius of 5.6 μm and without employing

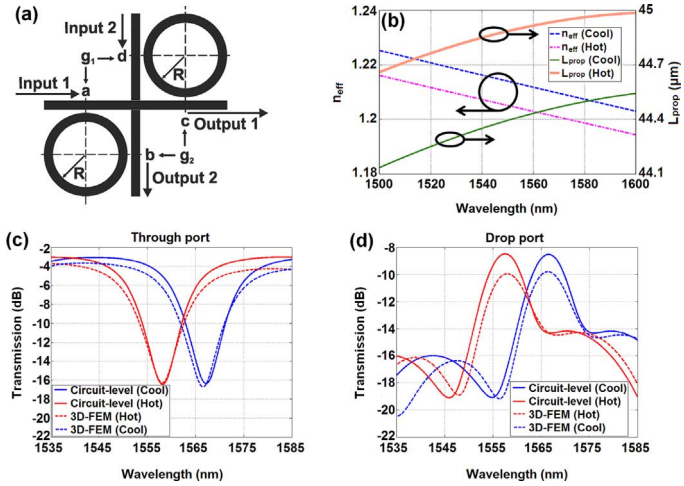

Fig. 5. (a) The 2×2 dual-ring DLSPP switch layout, (b) Effective refractive index and propagation lengths for a straight DLSPP waveguide according to FEM eigenmode analysis. Transmission spectra of (c) Through and (d) Drop ports in both heated and unheated states by using circuit-level (solid lines) and 3D-FEM analysis (dotted lines).

a racetrack design, so that both L_1 and L_2 equal zero. The gap dimensions employed in the 3D-FEM model have been 300 nm for the coupling stages a and d and 500 nm for the coupling stages b and c, respectively. The detailed material and geometrical parameters as well as the methodology adopted in the 3D-FEM analysis are documented in [25].

Figs. 5(c) and (d) illustrate the transmission spectra within the 1535–1585 nm window for the Through and Drop ports, respectively, obtained by means of circuit-level and 3D-FEM modeling, for the unheated ("Cool") and heated ("Hot") states when light enters the 2×2 switch arrangement via its input port 1. In that case, Through functionality is actually obtained at output port 1, while the dropped signal emerges at output port 2. As can be clearly noticed, the device response achieved through circuit-level analysis closely follows respective results obtained through detailed electromagnetic modeling of the complete dual-ring structure. The IL values for the Through and Drop ports when unheated are -3.1 dB and -8.5 dB, respectively, while the ER parameter for the unheated Through resonance at 1567.2 nm is 13.3 dB. The transmission at the Drop-port has again an irregular shape that is also different with respect to the corresponding spectra obtained by the dual-resonator DLSPP add/drop filter of Fig. 2. A clear transmission peak is again formed, however its adjacent minima reach different power levels yielding ER values of 10.6 dB and 5.8 dB for its left- and right hand-side dip, respectively. The broadband characteristics of this layout are again evident showing a -3 dB bandwidth of approximately 9.4 nm for the Drop peak and more than 9.1 dB suppression over a 6 nm band for the Through resonance.

Both figures demonstrate effective tuning of the Through- and Drop-port resonances when the dual-ring structure is heated, showing a wavelength shift of 9 nm. The thermo-optic coefficient (TOC) that has been used was -1.05×10^{-4} K^{-1} corresponding to PMMA. The applied temperature change of 100 K has been used so as to reside below the maximum service temperature of PMMA, although its operational limits in experimental PMMA-loaded SPP structures have not been explored so far. The power coupling coefficients employed in this design have been $\xi_a^2 = 0.32, \xi_b^2 = 0.28, \xi_c^2 = 0.28$ and $\xi_d^2 = 0.32$. The coefficients ξ_b^2 and ξ_c^2 used in this case for the coupling sections of 300 nm gaps are higher than the corresponding coefficients utilized in the add/drop filtering configuration for approximately the same coupling conditions, since the level of coupling in fabricated structures seems to be lower than that predicted by 3D-FEM analysis [22], [24].

These results have been obtained by calculating the dual-ring power transfer functions for two different n_{eff} values, one corresponding to the hot and one to the cool state. These values have relied on the n_{eff} curves obtained through FEM eigenmode analysis for a straight DLSPP waveguide with a gold stripe of 3 μm width and 60 nm thickness, applying again a negative offset in order to incorporate the bending- and coupling-induced contributions to the effective refractive index. Fig. 5(b) depicts the n_{eff} and propagation length values resulting from FEM eigenmode analysis both for the unheated and heated states, assuming an applied temperature change of $\Delta T = 100$ K and neglecting the material dispersion of gold, as done in [25]. The negative n_{eff} offset used in the circuit-level analysis has been the same for both the cool and hot operational states equaling 0.1.

IV. The SOI-MUX

The high FSR of the 2×2 dual-ring DLSPP switch design necessitated by the requirement for sustaining plasmonic propagation losses within acceptable limits, has a direct impact on the specifications of the preceding SOI-based channel multiplexing stage. Successful multi-wavelength operation of the switching module requires that all channels inputting the switch have to reside within the spectral passband of a single switch resonance. This means that aggregate traffic rates and throughput can only increase through respective reductions in the channel spacing, whose lower bound is, however, determined by the channel line-rate and its data format. In the case of 40 Gb/s NRZ optical data employed in the proposed router platform, the channel spacing should not be lower than 100 GHz in order to enable high quality signals at the MUX output.

The SOI-MUX device implementations reported so far have mainly relied on the interconnection of either first or higher order ring structures [36]–[40] or, alternatively, of asymmetric Mach–Zehnder interferometric configurations [6], usually employing thermal tuning for establishing ideal spectral positioning of the MUX resonances. Channel density has been, however, limited to channel spacing values higher than 200 GHz in all these demonstrations, rendering them inefficient in their incorporation in a Wavelength Division Multiplexed (WDM) silicon-plasmonic router platform with high throughput requirements. SOI-MUX designs in silicon-plasmonic routing architectures have to ensure maximum aggregate throughput over enhanced bandwidth utilization metrics, taking also into account that multiplexing of 40 Gb/s NRZ data requires a 3 dB passband bandwidth of at least 40 GHz.

This section describes the design of a 4×1 SOI-MUX device capable of multiplexing four individual optical NRZ data streams at 40 Gb/s line rates spaced by 100 GHz. The proposed layout is shown in Fig. 6(a) and comprises four cascaded second order SOI micro-ring resonators (MRs). Second-order

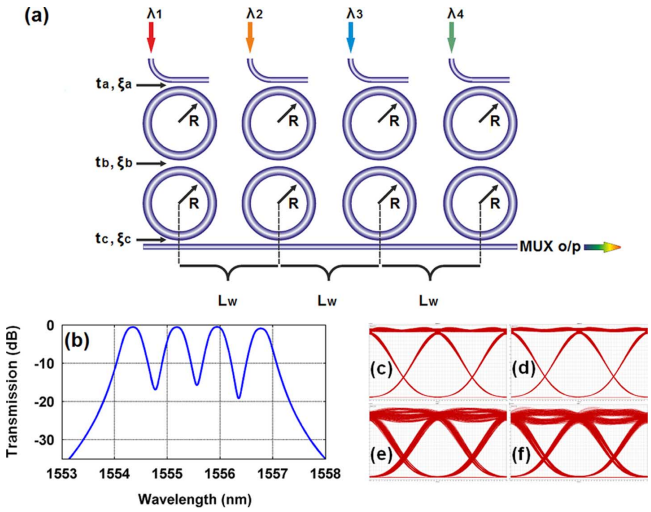

Fig. 6. (a) 4-channel MR SOI-MUX layout. Simulation results showing the (b) transfer function at common port for $R = 5.4\ \mu$m, (c)–(d) eye diagrams of channel #2, #3 before MUX, (e)–(f) eye diagrams of channel #2, #3 after MUX.

ring structures allow for increased flexibility in determining the spectral filtering shape and bandwidth of the MUX transmission peaks within the same channel spacing constraints due to the additional coupling stage employed between the two ring resonators [41]. All eight individual MRs have the same radius R and are considered as thermally tunable elements connected to electrical heating stages [42]. The waveguide distance between all neighboring second order rings is L_w. The optical power coupling coefficients between straight and ring waveguides are represented by ξ_a^2 and ξ_c^2 for the upper and lower ring, respectively, and by ξ_b^2 for the inter-ring coupling, having the same values for all four second order MR devices.

The first input signal at λ_1 wavelength is imported through the first second order MR, is exported to its Drop port and arrives at MUX output after travelling through the Add ports of the subsequent three cascaded rings. In a similar way, the second input signal at λ_2 wavelength emerges at the Drop port of the second MR structure and reaches the MUX output after propagating through the Add ports of the remaining two cascaded rings. The same procedure is repeated for λ_3 and λ_4 wavelengths entering the device through the subsequent second order MR modules, with the number of Add port transitions decreasing with increasing channel number. The optical signal finally exiting the MUX device is provided by the superposition of all four individual dropped channels stemming from the corresponding second order MR elements.

The electrical field transfer function for the second order MR Drop port is given by the well-known expression [41] (8), shown at the bottom of the page, while the respective transfer function for its Add port is provided by [41] (9), shown at the bottom of the page.

In (8) and (9), the index i denotes the rank of the second order MR in the cascade and can be any number between 1 and 4, R_i stands for its radius value, $L_{R_i} = 2\pi R_i$ represents the circumference of a single ring, and $\varphi_{R_i} = (2\pi/\lambda)(n_{\text{eff}} + \Delta n_i)L_{R_i}$ provides the phase shifting acquired during a ring roundtrip. The effective refractive index of the SOI waveguide is represented by n_{eff} and is assumed to be the same in straight and bending waveguide regions, while Δn_i stands for the effective refractive index change induced by heating. Moreover, (t_k, ξ_k) with $k = a, b, c$ denote the electrical field transmission and coupling coefficients corresponding to the optical power coupling and transmission factors (ξ_k^2, t_k^2) respectively, obviously satisfying the condition $t_k^2 + \xi_k^2 = 1$. The power propagation loss coefficient is given by a.

As the i-th incoming channel propagates through a single Drop-port filtering stage and through 4-i Add-port filtering functions, the complete SOI-MUX input-output transfer function for a single channel i is derived as:

$$H_{\text{channel}_i} = H_{D_i}(H_W)^{4-i}\left(\prod_{k=i+1}^{4} H_{A_k}\right) \tag{10}$$

with $H_W = \sqrt{e^{-aL_W}}e^{-j\varphi_W}$ being the transfer function of a single straight waveguide section of length L_w employed between successive second order MRs and $\varphi_W = (2\pi/\lambda)n_{\text{eff}}L_W$ providing the corresponding acquired phase.

Consequently, the total optical power transfer function of the SOI-MUX circuitry is obtained by the equation:

$$S_{o/p} = \left|\sum_{i=1}^{4} H_{\text{channel}_i}\right|^2 \tag{11}$$

Fig. 6(b) depicts the spectral response for a 4 × 1 SOI-MUX circuit for the case of a ring radius of 5.4 μm and for 100 GHz spaced resonances. The 100 GHz spacing between the resonances of successive second order ring structures is obtained by considering an effective refractive index change of Δn_i equal to approximately 0.0013 between them. This yields a maximum required effective refractive index change of 0.0038 exhibited between the first and last second order ring structure, which is within the range of electrically induced thermal resonance shifting in SOI ring configurations [42]. The ER between resonance maxima and minima is 15 dB, while the 3 dB bandwidth

$$H_{D_i} = \frac{-j\xi_a\xi_b\xi_c\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}}}{1 - t_at_b\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}} - t_bt_c\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}} + t_at_ce^{-aL_{R_i}}e^{-j2\varphi_{R_i}}} \tag{8}$$

$$H_{A_i} = \frac{t_c - t_at_bt_c\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}} - t_b\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}} + t_ae^{-aL_{R_i}}e^{-j2\varphi_{R_i}}}{1 - t_at_b\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}} - t_bt_c\sqrt{e^{-aL_{R_i}}}e^{-j\varphi_{R_i}} + t_at_ce^{-aL_{R_i}}e^{-j2\varphi_{R_i}}} \tag{9}$$

TABLE I
SOI-MUX MODELING PARAMETERS

N_{eff}	a	R	L_W	$\xi_a{}^2 = \xi_c{}^2$	$\xi_b{}^2$
2.428	2 dB/cm	5.4 μm	5.4π μm	0.06	0.0007

TABLE II
EFFECTIVE REFRACTIVE INDEX CHANGE IN SECOND ORDER RINGS

	$MR\ (\lambda_1)$	$MR\ (\lambda_2)$	$MR(\lambda_3)$	$MR(\lambda_4)$
Δ_{n_i}	0	0.0013	0.0025	0.0038

of each resonant peak equals 42 GHz. The optical power coupling factors between straight-ring (ξ_a^2, ξ_c^2) and ring-ring waveguides (ξ_b^2) are relatively low, equaling 0.06 and 0.0007, respectively, being again within the gap distance fabrication capabilities of state-of-the-art SOI technology. The distance between cascaded rings has been equal to $L_W = \pi R$, which has been found to provide the optimal phase matching conditions towards maximizing the extinction ratio values and at the same time ensuring a high 3 dB resonant bandwidth. Besides, this distance is large enough to assure that no coupling between rings in the horizontal direction occurs. The set of parameters used for this SOI-MUX configuration as well as the variation of effective refractive index for each stage of cascaded second order MR are summarized in Tables I and II, respectively.

The signal degradation induced by this SOI-MUX design has been evaluated by means of a co-operative simulation framework between the SOI-MUX model and the commercially available VPI Photonic simulation suite. Figs. 6(c)–(d) depict the eye diagrams for channels #2 and #3 at approximately 1555.2 nm and 1556 nm before entering the SOI-MUX layout and being modulated with 40 Gb/s Pseudorandom Binary Sequence (PRBS) $2^7 - 1$ NRZ data signals. Figs. 6(e)–(f) illustrate the respective eye diagrams at the output of the SOI-MUX circuit. Slight signal quality degradation in terms of timing and amplitude jitter can be observed at the SOI-MUX output; however a clearly open eye is still obtained in all cases, indicating that this signal can be effectively used in subsequent processing stages.

V. DLSPP-TO-SI-RIB TRANSITION

This section describes the coupling design used for efficiently interfacing the silicon and plasmonic waveguides. Interfacing these two technologies will allow for exploiting low-loss silicon-based circuitry for passive operations and utilizing the high-loss DLSPP structures only where high tunability is required in a complex router architecture setup. An approach for coupling light from silicon-to-DLSPP waveguides and *vice versa* has been recently experimentally demonstrated in [27] based on butt-coupling. However, the silicon waveguide dimensions used in that implementation are not suitable for complex SOI-based passive configurations like the SOI-MUX circuitry.

In this work, the silicon layer of the SOI-side rib waveguide has a thickness of 340 nm at the guiding ridge that is not etched down all the way to the oxide-buffer layer, leaving a 50 nm-thick silicon slab. The SOI-side waveguide is coated with Spin-On-Glass (SOG), a necessary practice when heating stages at different sections of the SOI platform are used, as for example in the case of SOI-MUX circuitry. Fig. 7 depicts a side-view of the simulated structure. The waveguide cross-sections are also depicted as insets. A longitudinal metallic film gap is introduced aiming to ensure fabrication reproducibility while taking into account possible resolution limitations. This gap value is initially set to 0.5 μm.

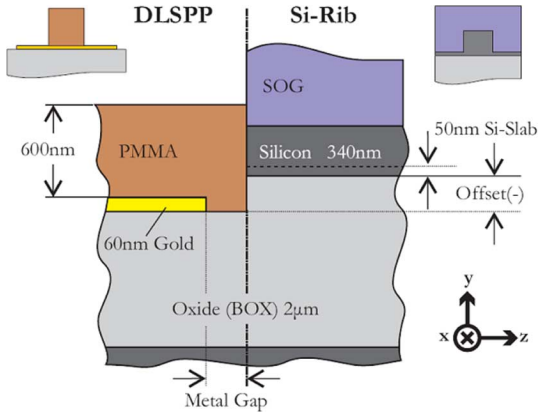

Fig. 7. Side view (zy-plane) of the DLSPP-to-Si-Rib waveguide transition along with the principal geometrical parameters.

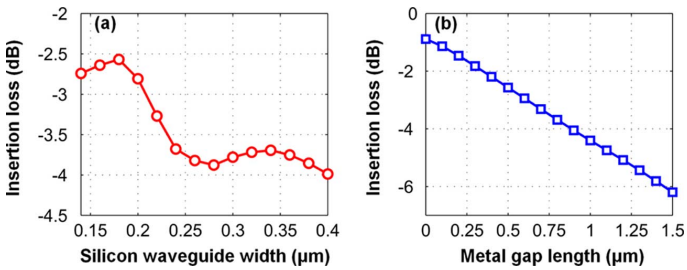

Fig. 8. Parametric study of the DLSPP-to-Si-rib waveguide transition. (a) Insertion loss versus silicon waveguide width. The vertical offset is set at its optimum (200 nm) and the metal gap is 0.5 μm long. (b) Insertion loss versus metal gap length. Both silicon waveguide width and vertical offset are set at their optimal values: 180 and 200 nm, respectively.

Numerical modeling is conducted by means of vectorial 3D-FEM simulations. Both the vertical offset and the silicon waveguide width were varied for coupling optimization. Minimum insertion losses (IL) were observed for a width value of 180 nm along with an offset of 200 nm. Specifically, the IL at this optimum point in width-offset space is approximately 2.6 dB (Fig. 8). Fig. 8(a) depicts the IL variation with respect to silicon waveguide width with the vertical offset fixed at its optimum value (200 nm). Width values smaller than 140 nm are not examined since for such values the fundamental TM mode of the Si-rib waveguide severely lacks confinement and eventually becomes leaky. The no-tapering penalty, i.e., the loss penalty in case the silicon waveguide is left at its nominal width (400 nm), is approximately 1.4 dB. On the other hand, the no-offset penalty, i.e., the loss penalty in case no vertical offset is provided, is somewhat smaller: approximately equal to 1 dB. Finally, the influence of the gap length on the insertion loss is investigated for the optimum case. The gap length is varied from 0 to 1500 nm and the results are depicted in Fig. 8(b). Insertion losses remain smaller than 4 dB for gaps up

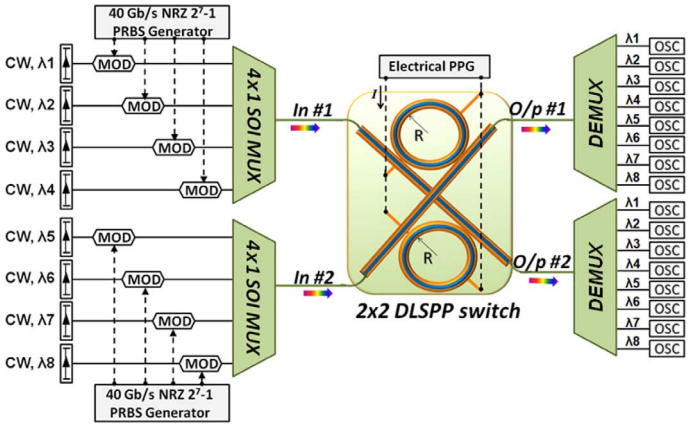

Fig. 9. Layout of the 2 × 2 silicon-plasmonic 320 Gb/s router.

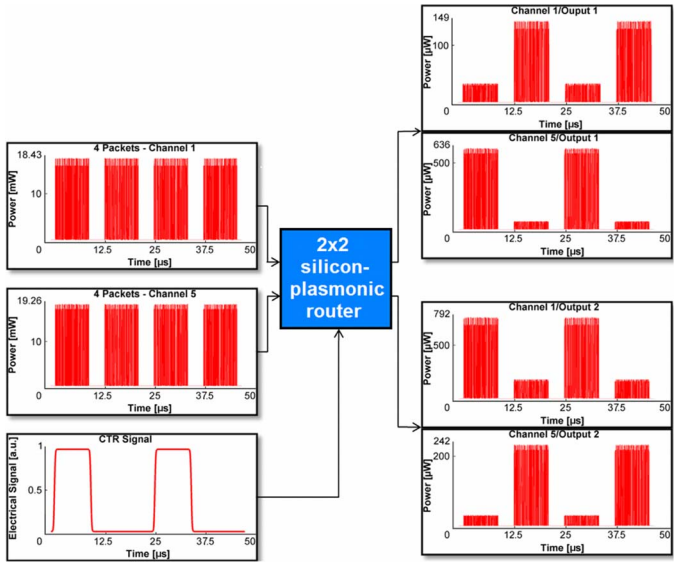

Fig. 10. Overview of 2 × 2 silicon-plasmonic time domain routing performance with ch #1 and #5 injected into the router.

to 900 nm. On the other hand, the ideal case of zero gap leads to an insertion loss of 1 dB. Similar results have been obtained for the Si-Rib-to-DLSPP transition.

VI. 2 × 2 Router Performance

The obvious benefits of reliable circuit-level modeling for both the DLSPP and SOI-based configurations compared to corresponding FEM approaches involve the important savings in time and computational power requirements. Even more important, circuit-level models can be incorporated in more sophisticated optical network simulation tools, so that the performance of complex silicon-plasmonic router layouts can be evaluated. Fig. 9 shows the proposed 2 × 2 silicon-plasmonic router architecture that has been evaluated through simulations by means of the commercially available VPI photonic component library, properly incorporating the circuit-level models for the 2 × 2 dual-ring DLSPP switch and the SOI-MUX circuit. Eight 100 GHz-spaced 40 Gbps $2^7 - 1$ PRBS NRZ data packet modulated wavelength channels grouped in two 4-wavelength clusters are launched into the two 4 × 1 SOI-MUX modules. These SOI-MUX circuits rely on the design described in Section IV and have used a ring radius of 5.4 μm and 5 μm, respectively, so as to operate in two different spectral regions and allow for the multiplexing of the two 4-wavelength data signal clusters. Therefore, the output of each MUX yields a 4-wavelength data stream carrying an aggregate traffic of 160 Gb/s. Subsequently, the two SOI-MUX output signals enter a 2 × 2 dual-ring PMMA-loaded SPP switch, so that In #1 stream comprises channels #1 to #4 while In #2 stream involves channels #5 to #8. The DLSPP switch is identical to the one described in Section III.C and depicted in Fig. 5(a). The Si-Rib-to-DLSPP coupling interfaces have been taken into account as loss coefficients with 2.6 dB loss per facet.

Fig. 10 shows time domain simulation results for the evaluation of the 2 × 2 DLSPP based router, depicting the packet-formatted traffic of channels #1 and #5 when entering the switch through input ports 1 and 2, respectively. The data packets have a duration of 8.75 μsec and inter-packet guardbands of 3.5 μsec. The guardband time-window requirements are enforced by the on-off switching time of the thermo-optic DLSPP structure that has been assessed by means of 3D-FEM, taking into account the thermal diffusion equation [22]. The respective values that have been obtained for the 10%–90% rise- and fall-time of the temporal switch response when being thermally excited by a rectangular electrical pulse have been found to be 1.62 μsec and 1.82 μsec, respectively. This temporal behavior has been taken into account in the router evaluation by means of the electrical control pulse sequence used for driving the DLSPP switch, which considers electrical pulses of 10.5 μsec duration with rise- and fall-times equal to the respective values of the thermally induced on-off switching characteristics. As shown in Fig. 10, a periodic electrical pulse waveform with a period of 24.5 μsec has been used so as to have the DLSPP switch operating in its CROSS state when packets #1 and #3 are entering the dual-ring structure, while operating in its BAR state for packets #2 and #4.

Fig. 11(a) depicts the eye diagrams of channels #2, #3, #6 and #7 at output 1 of the DLSPP switch. Corresponding eye diagrams of these channels at output 2 are illustrated at Fig. 11(b). Similar eye diagrams are also obtained for channels #1, #4, #5 and #8. Figs. 11(c)–(d) illustrate the spectra of the signal emerging at switch output #1 and #2, respectively, both when operating in its OFF (BAR)-state and its ON (CROSS)-state, which correspond to unheated (20°C) and heated rings (120°C). ER values obtained between ON and OFF switching states at output #1 for all 8 channels vary from 5.9 dB for channel #1 up to 9.5 dB for channel #5. Similar ER values are obtained at output port #2 that lie in the range from 5.1 dB for channel #8 to 8.8 dB for channel #4. ER values measured via the eye diagram curves between logical "1" and logical "0" for all channels at both output ports range from 5 dB to 10 dB and are presented in Fig. 11(e)–(f). The total loss of the router layout has been found to be close to 15 dB.

This performance evaluation has relied on the assumption that the PMMA-loaded dual-ring SPP structure can be heated up to 120°C, allowing for a temperature change of 100 K in order to enable a wavelength shift of 9 nm. It should be, however, noted

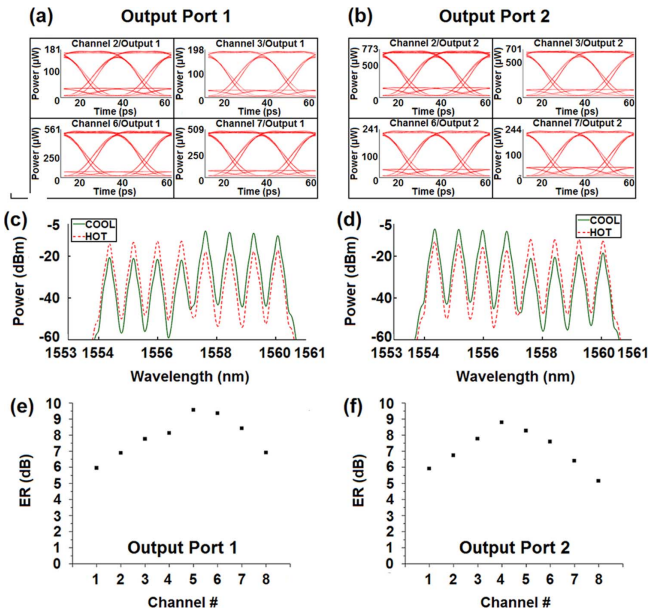

Fig. 11. Simulation results showing the eye diagrams of ch #2, #3, #6 and #7 at Output Ports 1(a) and 2(b), spectra of multi-wavelength signal obtained at Output Ports 1(c) and 2(d), ER values for each channel at Output Ports 1(e) and 2(f), respectively, when the switch is the ON or OFF states.

that the same or even improved performance could be in principle obtained by considering a different polymer-loading with higher thermo-optic coefficient than PMMA. As such, the use of a higher TOC polymer would not affect the transfer function characteristics of our router platform in both its CROSS and BAR operating states, but could allow for reduced heating requirements in order to reach similar, or even larger, wavelength shifts.

VII. Conclusion

We have demonstrated a 2×2 high-throughput silicon-plasmonic router architecture for high capacity optical interconnect applications, using a dual-ring DLSPP device as the 2×2 switching module and a SOI-MUX design for creating multi-wavelength data packet streams. We have presented experimental results of a novel dual-resonator DLSPP structure when operating as a passive optical add/drop filtering element and simulation-based results through rigorous 3D-FEM analysis when performing as a 2×2 thermo-optic switch. The frequency-domain transfer function of this device is derived and has been used for efficient circuit-level modeling of dual-resonator DLSPP architectures, agreeing with both the experimental and the 3D-FEM modeling results. Moreover, a 4×1 SOI-MUX circuit design relying on cascaded second order rings has been presented, demonstrating successful performance for 40 Gb/s NRZ channel multiplexing in the case of 100 GHz channel spacing requirements. The silicon-to-DLSPP waveguide transition has been implemented via a butt-coupling approach and the optimal interface-structure parameters have been defined through 3D-FEM, showing that coupling loss values of 2.6 dB can be obtained. The 2×2 dual-ring DLSPP switch and the SOI-MUX circuit-level models have been then incorporated into a co-operative simulation environment relying on the VPI simulation platform, forming a 2×2 silicon-plasmonic router architecture that has been evaluated for 8-channel data packet traffic of 320 Gb/s aggregate rate. The performance of this router configuration has been found successful for all employed channels, showing that ER values higher than 5 dB can be obtained. To this end, the proposed router architecture could allow for effective footprint and power consumption reduction in optical interconnect routing platforms, using low-loss silicon photonics for passive circuit functionalities and exploiting the small-size and low-energy plasmonics when switching functionality is targeted.

Acknowledgment

The authors would like to acknowledge Dr. M. Baus, Dr. M. Karl, and Dr. T. Tekin for useful discussions.

References

[1] D. A. B. Miller, "Optical interconnects," in *Proc. Opt. Fiber Commun. Conf.*, San Diego, CA, Mar. 2010, Tutorial OThX1.
[2] P. K. Pepeljugoski, "Low-power and high-density optical interconnects for future supercomputers," in *Proc. Opt. Fiber Commun. Conf.*, San Diego, CA, Mar. 2010, paper OThX2.
[3] R. Luijten and R. Grzybowski, "The osmosis optical packet switch for supercomputers," in *Proc. Opt. Fiber Commun. Conf.*, San Diego, CA, Mar. 2009, paper OTuF3.
[4] W. Bogaerts *et al.*, "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," *J. Lightw. Technol.*, vol. 23, no. 1, pp. 401–412, Jan. 2005.
[5] B. Jalali, "Teaching silicon new tricks," *Nature Photon.*, vol. 1, no. 4, pp. 193–195, Apr. 2007.
[6] A. Liu *et al.*, "Wavelength division multiplexing based photonic integrated circuits on silicon-on-insulator platform," *IEEE J. Sel. Topics Quantum Electron*, vol. 16, no. 1, pp. 23–32, Jan./Feb. 2010.
[7] A. Alduino *et al.*, "Demonstration of a high speed 4-channel integrated silicon photonics WDM link with hybrid silicon lasers," in *Proc. Integr. Photon. Res., Silicon and Nanophoton.*, Monterey, CA, Jul. 2010, paper PDIWI5.
[8] F. E. Doany, B. G. Lee, C. L. Schow, C. K. Tsang, C. Baks, Y. Kwark, R. John, J. U. Knickerbocker, and J. A. Kash, "Terabit/s-class 24-channel bidirectional optical transceiver module based on TSV Si carrier for board-level interconnects," in *Proc. Electron. Compon. Technol. Conf.*, Jun. 2010, pp. 58–65.
[9] A. Biberman, B. G. Lee, N. Sherwood-Droz, M. Lipson, and K. Bergman, "Broadband operation of nanophotonic router for silicon photonic networks-on-chip," *IEEE Photon. Technol. Lett.*, vol. 22, no. 12, pp. 926–928, Jun. 2010.
[10] A. Shacham, K. Bergman, and L. P. Carloni, "Photonic networks-on-chip for future generations of chip multiprocessors," *IEEE Trans. Comput.*, vol. 57, no. 9, pp. 1246–1260, Sep. 2008.
[11] J. Chan, G. Hendry, A. Biberman, and K. Bergman, "Architectural exploration of chip-scale photonic interconnection network designs using physical-layer analysis," *J. Lightw. Technol.*, vol. 28, no. 9, pp. 1305–1315, May 2010.
[12] D. Vantrease *et al.*, "Corona: System implications of emerging nanophotonic technology," in *Proc. 35th Int. Symp. Comput. Arch.*, Beijing, China, Jun. 2008, pp. 153–164.
[13] R. Morris and A. K. Kodi, "Exploring the design of 64- and 256-core power efficient nanophotonic interconnect," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 5, pp. 1386–1393, Sep./Oct. 2010.
[14] R. Zia, J. A. Schuller, A. Chandran, and M. L. Brongersma, "Plasmonics: The next chip-scale technology," *Materials Today*, vol. 9, no. 7–8, pp. 20–27, Jul.–Aug. 2006.
[15] H. A. Atwater, "The promise of plasmonics," *Sci. Am. Mag.*, vol. 296, no. 4, pp. 56–63, Apr. 2007.
[16] D. K. Gramotnev and S. I. Bozhevolnyi, "Plasmonics beyond the diffraction limit," *Nature Nanophotonics*, vol. 4, no. 2, pp. 83–91, Feb. 2010.
[17] B. Steinberger *et al.*, "Dielectric stripes on gold as surface plasmon waveguides," *Appl. Phys. Lett.*, vol. 88, no. 9, Feb. 2006, Art. ID 094104.
[18] T. Holmgaard and S. I. Bozhevolnyi, "Theoretical analysis of dielectric-loaded surface plasmon-polariton waveguides," *Phys. Rev. B*, vol. 75, no. 24, Jun. 2007, Art. ID 245405.

[19] T. Holmgaard, Z. Chen, S. I. Bozhevolnyi, L. Markey, and A. Dereux, "Dielectric-loaded plasmonic waveguide-ring resonators," *Opt. Exp.*, vol. 17, no. 4, pp. 2968–2975, Feb. 2009.
[20] Z. Chen *et al.*, "Wavelength-selective directional coupling with dielectric-loaded plasmonic waveguides," *Opt. Lett.*, vol. 34, no. 3, pp. 310–312, Jan. 2009.
[21] T. Holmgaard, Z. Chen, S. I. Bozhevolnyi, L. Markey, and A. Dereux, "Design and characterization of dielectric-loaded plasmonic directional couplers," *J. Lightw. Technol.*, vol. 27, no. 24, pp. 5521–5528, Dec. 2009.
[22] O. Tsilipakos, T. V. Yioultsis, and E. E. Kriezis, "Theoretical analysis of thermally tunable microring resonator filters made of dielectric-loaded plasmonic waveguides," *J. Appl. Phys.*, vol. 106, no. 9, Nov. 2009, Art. ID 093109.
[23] J. Gosciniak *et al.*, "Thermo-optic control of dielectric-loaded plasmonic waveguide components," *Opt. Exp.*, vol. 18, no. 2, pp. 1207–1216, Jan. 2010.
[24] A. Dereux *et al.*, "Parametric study of dielectric loaded surface plasmon polariton add-drop filters for hybrid silicon/plasmonic optical circuitry," in *Proc. SPIE Photon. West* , San Francisco, CA, Jan. 2011, paper 7945-40.
[25] O. Tsilipakos, E. E. Kriezis, and S. I. Bozhevolnyi, "Thermo-optic microring resonator switching elements made of dielectric-loaded plasmonic waveguides," *J. Appl. Phys.*, vol. 109, no. 7, Apr. 2011, Art. ID 073111.
[26] J. Gosciniak, V. S. Volkov, S. I. Bozhevolnyi, L. Markey, S. Massenot, and A. Dereux, "Fiber-coupled dielectric loaded plasmonic waveguides," *Opt. Exp.*, vol. 18, no. 5, pp. 5314–5319, Feb. 2010.
[27] R. M. Briggs, J. Grandidier, S. P. Burgos, E. Feigenbaum, and H. A. Atwater, "Efficient coupling between dielectric loaded plasmonic and silicon photonic waveguides," *Nano Lett.*, vol. 10, no. 12, pp. 4851–4857, Oct. 2010.
[28] A. Kumar, J. Gosciniak, T. B. Andersen, L. Markey, A. Dereux, and S. I. Bozhevolnyi, "Power monitoring in dielectric-loaded surface plasmon-polariton waveguides," *Opt. Exp.*, vol. 19, no. 4, pp. 2972–2978, Feb. 2011.
[29] J. T. Kim *et al.*, "Chip to chip optical interconnect using gold long-range surface plasmon polariton waveguides," *Optics Exp.*, vol. 16, no. 17, pp. 13133–13138, Aug. 2008.
[30] T. Holmgaard, J. Gosciniak, and S. I. Bozhevolnyi, "Long-range dielectric-loaded surface plasmon-polariton wavelengths," *Opt. Exp.*, vol. 18, no. 22, pp. 23009–23015, Oct. 2010.
[31] O. Liboiron-Ladouceur *et al.*, "The data vortex optical packet switched interconnection network," *J. Lightw. Technol.*, vol. 26, no. 13, pp. 1777–1789, Jul. 2008.
[32] W. Bogaerts, P. Dumon, D. V. Thourhout, and R. Baets, "Low-loss, low-cross-talk crossings for silicon-on-insulator nanophotonic waveguides," *Opt. Lett.*, vol. 32, no. 19, pp. 2801–2803, Sep. 2007.
[33] P. B. Johnson and R. W. Christy, "Optical constants of the noble metals," *Phys. Rev. B*, vol. 6, no. 12, pp. 4370–4379, Dec. 1972.
[34] T. Nikolajsen, K. Leosson, and S. I. Bozhevolnyi, "Surface plasmon polariton based modulators and switches operating at telecom wavelengths," *Appl. Phys. Lett.*, vol. 85, no. 24, pp. 5833–5835, Dec. 2004.
[35] G. Gagnon, N. Lahoud, G. Mattiussi, and P. Berini, "Thermally activated variable attenuation of long-range surface plasmon-polariton waves," *J. Lightw. Technol.*, vol. 24, no. 11, pp. 4391–4402, Nov. 2006.
[36] M. Geng, L. Jia, L. Zhang, L. Yang, P. Chen, and Y. Liu, "Compact four-channel reconfigurable optical add-drop multiplexer using silicon photonic wire," *Opt. Commun.*, vol. 282, no. 17, pp. 3477–3480, Sep. 2009.
[37] T. Barwicz *et al.*, "Reconfigurable silicon photonic circuits for telecommunication applications," in *Proc. SPIE*, Feb. 2008, vol. 6872, pp. 68720Z-1–68720Z-12.
[38] E. J. Klein, D. H. Geuzebroek, H. Kelderman, G. Sengo, N. Baker, and A. Driessen, "Reconfigurable optical add-drop multiplexer using microring resonators," *IEEE Photon. Technol. Lett.*, vol. 17, no. 11, pp. 2358–2360, Nov. 2005.
[39] P. Dong *et al.*, "Low power and compact reconfigurable multiplexing devices based on silicon microring resonators," *Opt. Exp.*, vol. 18, no. 10, pp. 9852–9858, Apr. 2010.
[40] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel silicon micro-resonator based filters for WDM applications," *Opt. Exp.*, vol. 15, no. 12, pp. 7489–7498, Jun. 2007.
[41] P. Saeung and P. P. Yupapin, "Generalized analysis of multiple ring resonator filters: Modeling by using graphical approach," *Optik-Int. J. Light Electron Opt.*, vol. 119, no. 10, pp. 465–472, Aug. 2008.
[42] N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, "Optical 4 × 4 hitless silicon router for optical networks-on-chip (NoC)," *Opt. Exp.*, vol. 16, no. 20, pp. 15915–15922, Sep. 2008.

Sotirios Papaioannou received the Diploma degree and M.Sc. degree in computer science from Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2008 and 2010, respectively, where he is currently working toward the Ph.D. degree.

His research areas focus on analysis, design, and simulation of photonic circuits and systems for high-speed optical interconnects.

K. Vyrsokinos, biography not available at the time of publication.

O. Tsilipakos, biography not available at the time of publication.

A. Pitilakis, biography not available at the time of publication.

K. Hassan, biography not available at the time of publication.

J.-C. Weeber, biography not available at the time of publication.

L. Markey, biography not available at the time of publication.

A. Dereux, biography not available at the time of publication.

S. I. Bozhevolnyi, biography not available at the time of publication.

A. Miliou, biography not available at the time of publication.

E. E. Kriezis, biography not available at the time of publication.

N. Pleros, biography not available at the time of publication.