Interfacing Dielectric-Loaded Plasmonic and Silicon Photonic Waveguides: Theoretical Analysis and Experimental Demonstration

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***Abstract*—A comprehensive theoretical analysis of end-fire coupling between dielectric-loaded surface plasmon polariton and rib/wire silicon-on-insulator (SOI) waveguides is presented. Simulations are based on the three-dimensional vector finite element method. The geometrical parameters of the interface are varied in order to identify the ones leading to optimum performance, i.e., maximum coupling efficiency. Fabrication tolerances about the optimum parameter values are also assessed. In addition, the effect of a longitudinal metallic stripe gap on coupling efficiency is quantified, since such gaps have been observed in fabricated structures. Finally, theoretical results are compared against insertion loss measurements, carried out for two distinct sets of samples comprising rib and wire SOI waveguides, respectively.**

***Index Terms*—Optical waveguide junction, dielectric-loaded plasmonic waveguide, silicon on insulator waveguides, finite element method.**

I. Introduction

PLASMONIC waveguides and waveguide-based components are attracting an ever-increasing interest in recent years [1]–[3]. An abundance of passive and active configurations have been examined, in pursuit of nanoscale dimensions (beyond the diffraction limit) and/or high energy efficiency, stemming from field enhancement at metal-dielectric interfaces. However, such desirable features come at a cost, namely, high propagation losses associated with field penetration in metal regions. Thus, significant effort has been directed in reducing or compensating for the inherent resistive losses of plasmonic waveguides, through elaborate geometrical/material configurations [4]–[6] or by introducing materials with gain [7], [8], respectively. Nevertheless, the high insertion loss (IL) of plasmonic components still remains the bottleneck of their performance. Therefore, a simple idea emerged [9]: using plasmonic components only where small footprint and/or high efficiency is required and leaving the interconnection of such components to low-loss photonic waveguides. In other words, hybrid plasmonic-photonic circuits, instead of all-plasmonic ones, are currently deemed the most promising approach for realizing efficient nanophotonic circuitry. Obviously, for such circuits to become a reality, efficient interfacing of plasmonic and photonic waveguides is a necessary prerequisite.

To date, several plasmonic-photonic waveguide transitions have been examined based on either end-fire or directional coupling schemes. In the first case, spatial matching of the mode profiles is what mainly determines coupling efficiency, whereas in the second, it is phase matching that becomes the primary concern, since phase-constant disparity limits the maximum possible power exchange. Initially, studies revolved around the stripe plasmonic waveguide, since it was the first 2D plasmonic waveguide, i.e., able to confine light in both transverse directions, to be extensively investigated. Coupling to standard silica fibers [10], [11] and planar dielectric waveguides [12], [13] were progressively considered. However, the long-range mode supported by the stripe plasmonic waveguide lacks strong lateral confinement and therefore cannot serve the purpose of densely integrated circuits. Thus, efforts have recently concentrated on plasmonic waveguides exhibiting stronger confinement [14]–[20]. Specifically, these include wire [14], slot [15], [16], hybrid silicon-plasmonic [17]–[19], and dielectric-loaded surface plasmon polariton (DLSPP) [20] waveguides.

Among the aforementioned plasmonic waveguides, the DLSPP is the most extensively investigated. It has been employed in the implementation of a broad range of passive as well as active components, primarily utilizing the thermo-optic effect [21]–[24]. Moreover, it is technologically simple and exhibits

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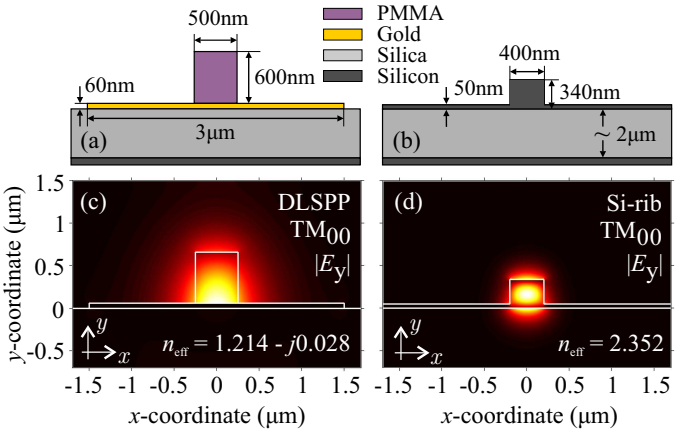

Fig. 1. (a) DLSPP and (b) Si-rib waveguide cross-sections. All dimensions are in scale except for the BOX thickness. Distribution of the dominant E-field component (absolute value) for (c) the fundamental quasi-TM mode of the DLSPP waveguide and (d) the fundamental quasi-TM mode of a 400-nm-wide Si-rib waveguide. The respective effective indices are also included.

relatively small propagation losses. Specifically, the propagation length, i.e., the e-folding distance of the optical intensity, is in the order of 50 μm for the fundamental TM_{00} mode. At first, an attempt to access DLSPP waveguides via standard single-mode fibers was made [25]. This allowed for accurate fiber-to-fiber characterization of DLSPP-based components [21]. Obviously, coupling to fibers does not serve the purpose of planar hybrid plasmonic-photonic circuits. Therefore, an end-fire approach for coupling light between DLSPP and planar silicon-on-insulator (SOI) waveguides has been recently demonstrated [20]. However, a thorough numerical investigation of the waveguide interface has yet to be performed. Moreover, the rib silicon waveguide of [20] is rather bulky and thus a different choice for the SOI waveguide could prove advantageous, provided, of course, that the coupling efficiency is equally good.

In this work, we thoroughly analyze the performance of end-fire coupling between the DLSPP and a compact SOI waveguide. Both rib and wire variants of the SOI waveguide are examined, and a comparison between the two is provided. In each case, the geometrical parameters of the interface are varied in order to identify the ones leading to optimum performance, i.e., maximum coupling efficiency or, equivalently, minimum insertion loss. Fabrication tolerances about these optimum parameter values are also quantified. In addition, we assess the effect of a longitudinal metallic stripe gap on insertion loss, since such gaps have been observed in fabricated samples. Finally, theoretical findings are compared against insertion loss measurements, carried out for two distinct sets of samples, comprising wire and rib SOI waveguides, respectively.

II. DLSPP and Si-Rib Waveguides

Fig. 1(a),(b) depicts the cross-sections of both DLSPP and Si-rib waveguides. Specifically, the DLSPP waveguide [Fig. 1(a)] consists of a 500 nm $\times$ 600 nm poly-methyl-methacrylate (PMMA) ridge on top of a 3 μm $\times$ 60 nm gold stripe. The combined structure of ridge and stripe resides on a typical silicon-on-insulator (SOI) substrate with a buried oxide (BOX) thickness of 2 μm (dimension not in scale). For such ridge dimensions, the DLSPP waveguide is single-mode at telecom wavelengths. On the other hand, the Si-rib waveguide consists of a 400 nm $\times$ 340 nm silicon core on top of the same SOI substrate. The height value of 340 nm ensures that the fundamental quasi-TM mode is well-confined. Outside the core region, the silicon layer is deeply etched leaving a 50-nm-thick silicon slab. Although not single-mode (the fundamental quasi-TE mode is also supported), the symmetry of the DLSPP mode field components dictates that coupling only to the fundamental quasi-TM mode of the Si-rib waveguide is actually possible. Finally, as far as the material parameters are concerned, the refractive indices of all materials involved at the working wavelength of 1.55 μm are: $n_{\mathrm{PMMA}} = 1.493$, $n_{\mathrm{Gold}} = 0.55 - j11.5$ [26], $n_{\mathrm{Silica}} = 1.45$, and $n_{\mathrm{Silicon}} = 3.45$.

In Fig. 1(c),(d) we plot the distribution of the dominant electric field component (E_y) for the fundamental quasi-TM modes of both waveguides. Clearly, spatial matching of the mode profiles is not particularly good. Specifically, the x-extent of the DLSPP mode is almost double that of the Si-rib mode. Furthermore, the two modes are not centered along the y-axis. As a result, the lower part of the Si-rib mode cannot contribute to coupling, since it is shadowed by the metallic stripe. Thus, it seems that both broadening the Si-rib mode along the horizontal (x) direction, as well as centering the two modes with respect to the vertical (y) direction are required in order to improve spatial matching. Broadening of the Si-rib mode can be actually accomplished by reducing the rib width, as this tends to relax mode confinement, whereas centering along the y direction can be provided by some kind of vertical offset between the two waveguides. Therefore, in what follows, certain dimensions of the interface are allowed to vary, in pursuit of optimum performance, i.e., maximum coupling efficiency or, equivalently, minimum insertion loss.

III. DLSPP to Si-Rib Waveguide Transition

In order to determine the coupling efficiency between the two waveguides (more specifically between their fundamental TM-like modes), we consider a DLSPP to Si-rib waveguide transition [Fig. 2(a)], meaning that light is impinging on the waveguide interface from the DLSPP waveguide. The opposite direction of propagation has been also examined, yielding identical (except for small differences of numerical origin) results. This is consistent with [27], which states that the coupling efficiency between two specific guided modes is reciprocal, even if other modes, guided or radiation ones, are excited at the interface. Note, however, that in such cases other quantities such as the return loss or total guided power, seize to be reciprocal [27].

All simulations of Sections III and IV are performed by means of an in-house implementation of the (frequency-domain) three-dimensional vector finite element method (3D-VFEM) [28]. Triangular prism elements and curl-conforming basis functions are utilized for discretizing the vector wave (curl-curl) equation. Standard first-order absorbing boundary conditions (ABCs) are implemented on the side walls, namely,

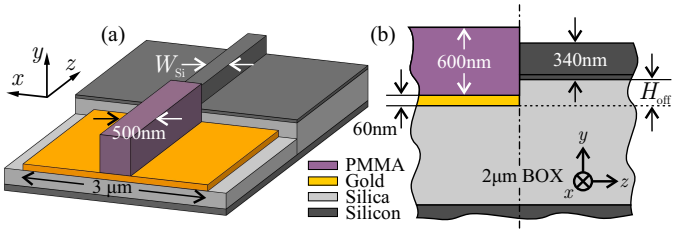

Fig. 2. Schematic of DLSPP to Si-rib waveguide transition without a longitudinal metallic stripe gap: (a) bird's eye view and (b) side view. The metallic stripe extends all the way to the waveguide interface.

xz and yz planes, for truncating the computational domain. However, extra care is exercised in implementing the ABC at the input waveguide port since the DLSPP mode is hybrid [29]. Note only that since this ABC is designed for a single guided mode, the input port must be placed sufficiently far away from the waveguide interface. For the same reason, the output waveguide is terminated with a perfectly matched layer (PML), instead of an ABC, since any radiation modes excited at the interface would not be properly absorbed by the ABC.

Let us now briefly comment on the procedure followed for calculating the coupling efficiency (insertion loss). Clearly, the DLSPP mode, besides exciting the fundamental guided mode of the Si-rib waveguide (TM_{00}), excites radiation modes as well. This is true especially for those geometrical parameter combinations leading to non-optimum spatial matching of the two TM_{00} modes. Therefore, while calculating the output power one should take extra care in distinguishing between the useful power carried by the TM_{00} Si-rib mode and power coupled to radiation modes which, obviously, should not enter in the result. For this purpose, a vector overlap integral of the following form

$$\frac{\left|\iint_A \mathbf{E}\times\mathbf{H}^*_{\mathrm{ref}}\cdot\hat{\mathbf{z}}\,dx\,dy\right|^2}{\left|\iint_A \mathbf{E}\times\mathbf{H}^*\cdot\hat{\mathbf{z}}\,dx\,dy\right|\left|\iint_A \mathbf{E}_{\mathrm{ref}}\times\mathbf{H}^*_{\mathrm{ref}}\cdot\hat{\mathbf{z}}\,dx\,dy\right|} \quad (1)$$

is evaluated along the output (Si-rib) waveguide. Specifically, at each z-coordinate the actual propagating field $\mathbf{E}(x,y;z)$ is correlated with a reference field $\mathbf{H}_{\mathrm{ref}}(x,y)$, namely, the TM_{00} Si-rib mode specified from the solution of a 2D eigenvalue problem of the waveguide cross-section, and properly normalized. The result of (1) is the fraction of the total guided power carried by the TM_{00} mode. Thus, by using this overlap integral to scale the total guided power, found by integrating the time-averaged Poynting vector over the waveguide cross-section, we can correctly determine the output power and, consequently, the insertion loss.

Finally, we note that in calculating the insertion loss of the waveguide junction, the propagation losses of the DLSPP mode are compensated for. This is done by artificially restoring the losses suffered during propagation in the DLSPP section of the waveguide transition under examination. The level of DLSPP propagation loss is specified from the solution of a 2D eigenvalue problem of the waveguide cross-section (imaginary part of effective index) and has been verified in an auxiliary 3D propagation problem of a single DLSPP waveguide. Thus, the reported insertion loss corresponds explicitly to the interface, which is considered lumped, and no particular reference to the waveguide lengths on either side is necessary.

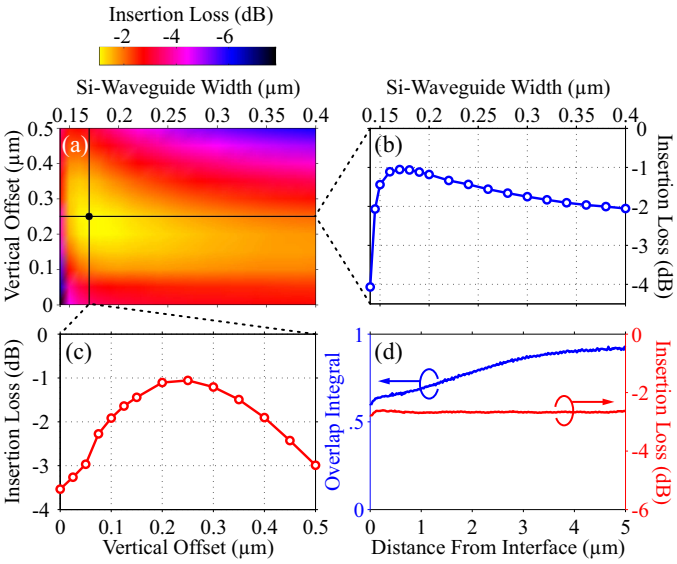

Fig. 3. Performance of DLSPP to Si-rib waveguide transition without a longitudinal metallic stripe gap: (a) Insertion loss (IL) as a function of Si-rib width (W_{Si}) and vertical offset (H_{off}). The optimum point in W_{Si}-H_{off} space is clearly marked and corresponds to (W_{Si}, H_{off}) = (170 nm, 250 nm). (b) IL vs W_{Si} for optimum value of H_{off}. (c) IL vs H_{off} for optimum value of W_{Si}. (d) Overlap integral and IL calculated along the output waveguide. W_{Si} is set at its nominal value (400 nm) and no vertical offset is provided. Although the overlap integral requires more than 5 μm of output waveguide length to approach unity, IL calculation can be safely performed even after less than 1 μm in the output waveguide.

A. *Without Longitudinal Metallic Stripe Gap*

We first focus on the simpler case that does not involve a longitudinal metallic stripe gap. This means that the metallic stripe extends all the way to the waveguide interface. A schematic of the simulated structure along with the relevant geometrical parameters is depicted in Fig. 2. In order to design an efficient transition, we have allowed for a vertical offset between the two waveguides. This offset, H_{off}, is simply the etch depth of the buried oxide layer in the DLSPP side of the transition [Fig. 2(b)]. To the same end, we have allowed for another degree of freedom, namely, the width of the silicon rib at the interface, W_{Si} [Fig. 2(a)]. We assume that the silicon waveguide is adiabatically tapered from the nominal width of 400 nm over a sufficiently long distance prior to reaching the interface, so as to ensure minimal tapering losses. The remaining geometrical parameters, namely, dimensions of PMMA ridge and gold stripe as well as silicon rib thickness, are fixed to their nominal values, already presented in Section II.

First, a parametric analysis with respect to both W_{Si} and H_{off} is performed, in order to identify the parameter values leading to optimum performance. The results are depicted in Fig. 3(a). Minimum insertion loss is attained for (W_{Si}, H_{off}) = (170 nm, 250 nm) and equals -1.05 dB. Such an IL value corresponds to a coupling efficiency of 80 %, equally good to the one reported in [20]. As anticipated, optimum performance

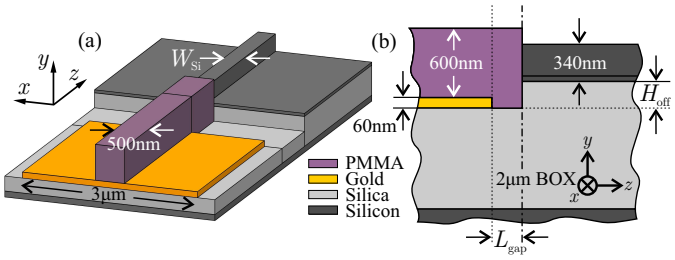

Fig. 4. Schematic of DLSPP to Si-rib waveguide transition with a longitudinal gap in the metallic stripe: (a) bird's eye view and (b) side view. Notice that the metallic stripe does not reach the waveguide interface.

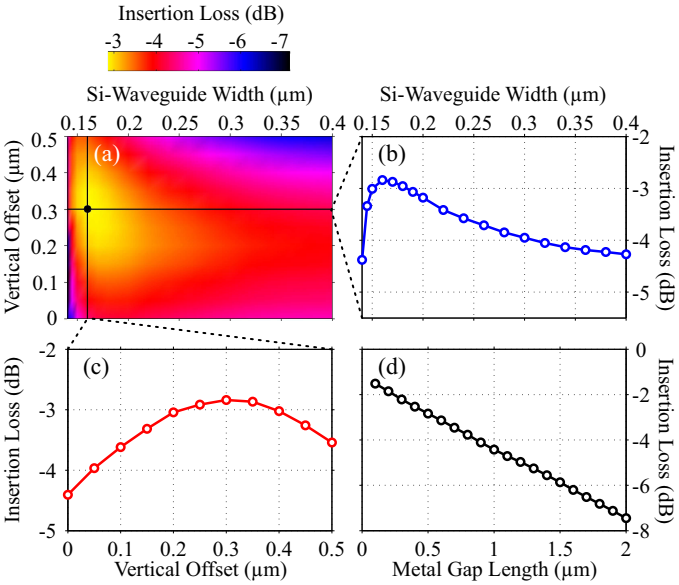

Fig. 5. Performance of DLSPP to Si-rib waveguide transition with a longitudinal metallic stripe gap: (a) Insertion loss (IL) as a function of Si-rib width ($W_{\rm Si}$) and vertical offset ($H_{\rm off}$). Metal gap length ($L_{\rm gap}$) is set to 0.5 μm. The optimum point in $W_{\rm Si}$-$H_{\rm off}$ space is clearly marked and corresponds to ($W_{\rm Si}$, $H_{\rm off}$) = (160 nm, 300 nm) (b) IL vs $W_{\rm Si}$ for optimum value of $H_{\rm off}$. $L_{\rm gap}$ is set to 0.5 μm. (c) IL vs $H_{\rm off}$ for optimum value of $W_{\rm Si}$. $L_{\rm gap}$ is set to 0.5 μm. (d) IL vs $L_{\rm gap}$ with $W_{\rm Si}$ and $H_{\rm off}$ set at their optimum values.

demands both reducing the Si-rib width, in order to broaden the supported mode, as well as providing a significant vertical offset, in order to center the modes vertically.

Next, we plot the IL as a function of each design parameter while keeping the other constant at its respective optimum [Fig. 3(b),(c)]. This way we can determine the fabrication tolerance about the optimum values. Specifically, Fig. 3(b) depicts the dependence on $W_{\rm Si}$ when $H_{\rm off}$ is at its optimum (250 nm). For widths ranging between $150-250$ nm the dependence is rather weak (IL remains better than -1.5 dB), indicating ample fabrication tolerance. The no-tapering penalty, i.e., the extra IL suffered should the waveguide width be left at its nominal value (400 nm), is 1 dB. We should also note that the steep IL increase for widths below 145 nm is due to the fact that for such widths the supported mode severely lacks confinement and eventually becomes leaky.

In the same way, Fig. 3(c) depicts the dependence on $H_{\rm off}$ when $W_{\rm Si}$ is fixed at its respective optimum (170 nm). Again, fabrication tolerance is ample. Specifically, IL remains better than -1.5 dB for vertical offsets ranging between $150-350$ nm. The no-offset penalty, i.e., the extra IL suffered in case no vertical offset is provided, is 2.5 dB. Let us also note that the abrupt jump in IL when the vertical offset exceeds the value of 60 nm (equal to metal stripe thickness) is associated with the lower part of the Si-rib mode contributing to coupling.

As discussed earlier, by following a procedure involving the computation of a vector overlap integral given by (1), we can safely calculate the insertion loss at almost any point along the output waveguide, even if radiation modes are still present. This is demonstrated in Fig. 3(d) depicting the overlap integral and insertion loss along the output waveguide. The Si-rib waveguide is left at its nominal width (400 nm) and no vertical offset is provided. Spatial matching of the two $\rm TM_{00}$ modes is not particularly good, leading to the excitation of radiation modes and yielding an insertion loss of approximately 2.7 dB. More than 5 μm in the output waveguide are required for the radiation modes to leave the computational domain and the overlap integral to approach unity. However, even less than a micrometer away from the waveguide interface the insertion loss can be safely calculated.

Regarding reflection from the interface, the 3D-FEM solution permits a rigorous calculation of the reflection coefficient associated with the fundamental mode of the input waveguide. Typical amplitude reflection coefficients for offsets and widths ranging from nominal to optimum values vary from 0.15 to 0.26. These values set corresponding upper limits on the insertion loss varying from -0.1 to -0.3 dB. Coupling to radiation modes and (to a much lesser extent) edge SPPs guided along the metallic stripe border are responsible for the actual IL not reaching the aforementioned values. For example, in the optimum case where coupling efficiency is 80 %, approximately 4 % of the impinging power is reflected from the interface in the form of the fundamental mode, whereas the remaining 16 % is mainly lost to radiation modes. Let us finally note that in general higher amplitude reflection coefficients (as high as 0.5) have been observed with the opposite propagation direction.

B. With Longitudinal Metallic Stripe Gap

In this Section, the DLSPP to Si-rib transition is slightly modified in order to include a longitudinal gap in the metallic stripe (Fig. 4). Specifically, the metallic stripe does not extend all the way to the waveguide interface but stops a distance $L_{\rm gap}$ before it [Fig. 4(b)]. Such gaps have been observed in fabricated samples. It is therefore expedient to assess their effect on insertion loss. Initially, this gap is set to 0.5 μm.

As was the case in Section III-A, first the optimum point in $W_{\rm Si}$-$H_{\rm off}$ space is sought. According to Fig. 5(a) this point corresponds to ($W_{\rm Si}$, $H_{\rm off}$) = (160 nm, 300 nm) and the respective IL is -2.85 dB. One notices that the optimum design parameters differ slightly from those of the previous Section (III-A) dealing with the no-gap variant of the waveguide junction. The different vertical offset optimum can be easily understood. While traversing the gap, the propagating field is lifted from the bottom of the ridge, since no metal/dielectric interface is any longer present, and tends to occupy its center. Therefore,

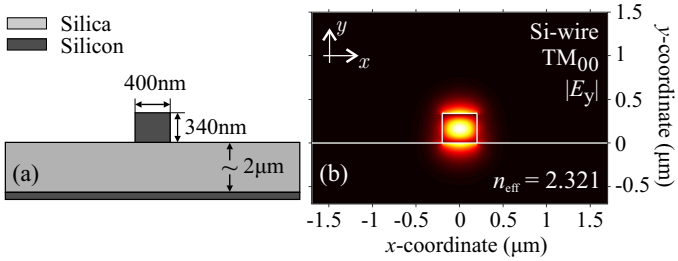

Fig. 6. (a) Cross-section of a 400-nm-wide Si-wire waveguide. (b) Distribution of the dominant E-field component (absolute value) for the corresponding TM_{00} mode. The distribution is very similar with that of the rib variant [cf. Fig. 1(d)].

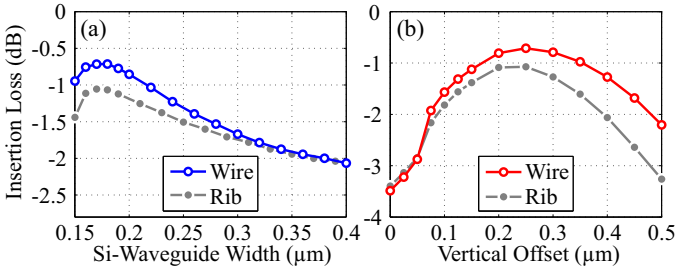

Fig. 7. Performance of DLSPP to Si-wire waveguide transition without a longitudinal metallic stripe gap: (a) IL vs W_{Si} for optimum value of H_{off} (250 nm). (b) IL vs H_{off} for optimum value of W_{Si} (180 nm). IL curves corresponding to Si-rib waveguides of identical dimensions are also included for comparison purposes.

the effective offset between modes at the waveguide interface will be somewhat smaller than the waveguide offset specified and thus a larger H_{off} value is now required. Moreover, while traversing the gap, the x-extent of the field components increases, explaining the different Si-rib-width optimum. This comes as no surprise, since the waveguide formed by the 500 nm $\times$ 660 nm polymer ridge on top of a silica substrate cannot sustain a guided mode. As a result, field components are bound to spread over the extent of the gap. Obviously, this explains the increased insertion losses (compared to the no-gap variant) as well.

Next, the IL dependence on each design parameter is separately examined. In Fig. 5(b) we plot the IL as a function of W_{Si}, while keeping H_{off} fixed at its optimum (300 nm). Again, the dependence around the optimum is not particularly strong. Specifically, for width values ranging between $150 - 220$ nm insertion loss remains better than -3.2 dB. The no-tapering penalty is slightly higher compared to the no-gap variant: approximately 1.4 dB. In the same way, Fig. 5(c) depicts the dependence on H_{off} when W_{Si} is fixed at its own optimum (160 nm). For etch depths ranging between $150 - 450$ nm the IL drops by less than 0.5 dB, indicating ample fabrication tolerance. The no-offset penalty in this case is approximately 1.6 dB. Note that this time there is no abrupt jump in IL [cf. Fig. 3(c)], since the metallic stripe does not reach the waveguide interface.

Finally, we investigate the effect of the longitudinal gap length (L_{gap}) on IL. We fix both W_{Si} and H_{off} at their optima (160 nm and 300 nm, respectively) and vary the gap length from 100 to 2000 nm. The results are depicted in Fig. 5(d). Insertion loss remains better than -5 dB for gaps as long as 1200 nm. For decreasing gap lengths, IL approaches the value of -1.15 dB, consistent with the one calculated for the no-gap variant with identical geometrical parameter values.

IV. DLSPP to Si-Wire Waveguide Transition

Let us now focus on a wire variant of the SOI waveguide. The silicon core dimensions are identical with those of the rib waveguide considered thus far, namely, 400 nm $\times$ 340 nm. The only difference is that outside the waveguide core, the silicon layer is etched all the way down to the oxide, leaving no remaining slab. Fig. 6 depicts the Si-wire waveguide cross-section along with the fundamental TM_{00} mode it supports. Clearly, the distribution of the dominant electric field component is very similar with that of the rib variant [cf. Fig. 1(d)], as one would probably expect given the rather small silicon slab height (50 nm). Therefore, the coupling efficiency for the DLSPP to Si-wire waveguide transition is anticipated to closely follow the one determined for the transition involving the rib waveguide, at least for the nominal value of core width (400 nm).

A. Without Longitudinal Metallic Stripe Gap

We first consider a no-gap DLSPP to Si-wire waveguide transition and follow a procedure identical to that of Section III-A for its analysis. First, the optimum point in W_{Si}-H_{off} space is identified. It corresponds to (W_{Si}, H_{off}) = (180 nm, 250 nm) and the respective IL equals -0.7 dB (coupling efficiency of 85 %). This constitutes a 0.35-dB improvement with respect to the rib case. Next, the IL dependence on each design parameter is separately examined. In Fig. 7(a) we plot the IL as a function of W_{Si}, while keeping H_{off} fixed at its optimum (250 nm). In the same way, Fig. 7(b) depicts the dependence on H_{off} when W_{Si} is fixed at its own optimum (180 nm). Insertion loss curves corresponding to the rib variant of the transition (identical geometrical parameters) are included for comparison purposes.

By observing Fig. 7(a) one can verify that for the nominal core width the two SOI waveguide variants yield almost identical insertion losses. This comes as no surprise since for large core widths the mode profiles of wire and rib variants are very similar, as mentioned earlier. However, for smaller widths the absence of a silicon slab has a stronger impact on field distribution. Fig. 8 depicts the distribution of the dominant electric field component for 170-nm-wide wire and rib SOI waveguides, respectively. Clearly, the mode distribution differs significantly, explaining the different coupling efficiencies in narrow SOI waveguide cases (Fig. 7).

B. With Longitudinal Metallic Stripe Gap

Let us now examine a DLSPP to Si-wire waveguide transition with a 0.5-μm-long metallic stripe gap. Parametric analysis reveals that the optimum point in W_{Si}-H_{off} space is (160 nm, 350 nm) and the respective IL equals -2.1 dB. Again, the performance of the wire waveguide is superior

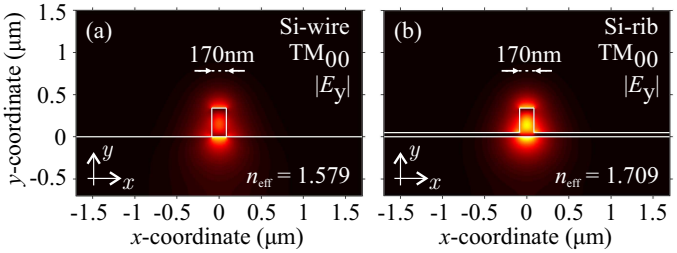

Fig. 8. Dominant electric field component distribution for the fundamental quasi-TM modes of 170-nm-wide (a) Si-wire and (b) Si-rib waveguides. The distributions are quite different for such small width values.

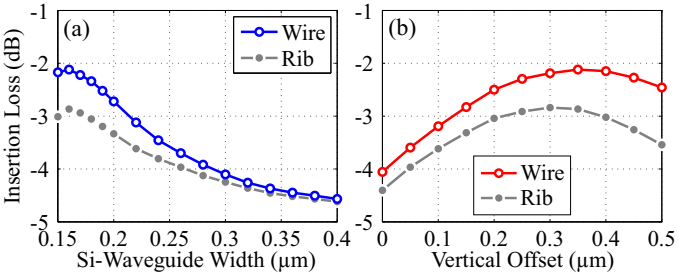

Fig. 9. Performance of DLSPP to Si-wire waveguide transition with a 0.5-μm-long metallic stripe gap: (a) IL vs W_{Si} for optimum value of H_{off} (350 nm). (b) IL vs H_{off} for optimum value of W_{Si} (160 nm). IL curves corresponding to Si-rib waveguides of identical dimensions are also included for comparison purposes.

TABLE I
OPTIMUM (W_{Si},H_{off}) POINTS AND RESPECTIVE INSERTION LOSS FOR ALL VARIANTS OF THE DLSPP-TO-SOI WAVEGUIDE TRANSITION EXAMINED.

	Optimum (W_{Si}, H_{off}) Point	Insertion Loss
Rib, without gap	(170 nm, 250 nm)	-1.05 dB
Rib, 0.5-μm gap	(160 nm, 300 nm)	-2.85 dB
Wire, without gap	(180 nm, 250 nm)	-0.70 dB
Wire, 0.5-μm gap	(160 nm, 350 nm)	-2.10 dB

compared to that of the rib; the insertion loss improvement is 0.75 dB. Moreover, as was the case with the rib variant of the waveguide transition (Section III), the optimum geometrical parameters are slightly different compared to the no-gap case. We have already noted in Section III-B that this is due to the evolution of the DLSPP mode along the gap.

In Fig. 9(a) we plot the IL as a function of W_{Si}, while keeping H_{off} fixed at its optimum (350 nm). Note once more that for the nominal value of core width (400 nm) the two SOI waveguide variants yield almost identical coupling efficiencies. On the other hand, this is not true for smaller widths. Fig. 9(b) depicts the dependence on H_{off} when W_{Si} is fixed at its optimum (160 nm). Evidently, for such a width value the wire variant significantly outperforms the rib.

Finally, in Table I we compile the optimum (W_{Si},H_{off}) points and respective insertion losses for all variants of the DLSPP-to-SOI waveguide transition examined in this work.

V. EXPERIMENTAL RESULTS

Following the design of the waveguide interface, samples comprising both wire and rib SOI waveguides were fabricated in order to verify the theoretical findings of Sections III and IV.

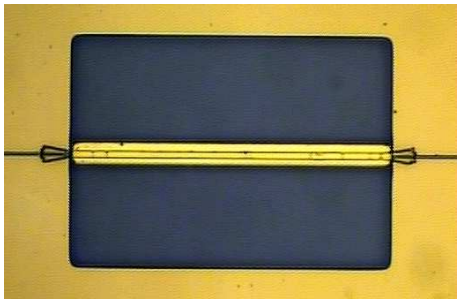

Fig. 10. Microscope image of a straight DLSPP waveguide coupled to access Si-wire waveguides. The cavity providing the necessary vertical offset between the two waveguides is clearly visible. PMMA funnel structures were introduced in both waveguide transitions to mitigate the deleterious effect of possible waveguide misalignments.

A. Sample Preparation

Plasmonic waveguide structures, including straight DLSPP waveguides and DLSPP-based components such as add-drop waveguide-ring-resonator (WRR) filters, were fabricated on SOI substrates. First, properly-situated access silicon waveguides were realized by electron beam lithography (EBL), using hydrogen silsesquioxane (HSQ) as a negative tone resist and hydrogen bromide (HBr)-based reactive ion etching (RIE). Then, substrates were recessed by means of a wet chemical etching process, so as to provide the necessary vertical offset between SOI and DLSPP waveguides, as determined from the theoretical analysis of Sections III and IV. Subsequently, the DLSPP waveguide circuits were formed. Gold stripes supporting the polymer (PMMA) loading were realized using a lift-off process based on a 1-μm-thick Clariant AZ nLOF photoresist patterned by 365 nm (I-line) exposure. Approximately 3 nm of Chromium (adhesive layer) and 60 nm of gold were deposited on the samples by thermal evaporation, followed by lift-off in N-Methyl-2-pyrrolidone (NMP) solvent. Then, a 600-nm-thick layer of PMMA resist was spin-coated on top of the samples. The waveguide mask was aligned and exposed using a 1850 mJ/cm^2 dose of 250-nm light. Samples were finally developed in methyl isobutyl ketone. UV lithography steps for both gold stripes and PMMA ridges were performed with a Süss Microtech MJB4 mask aligner equipped with a Hg/Xe arc source and exploited in the vacuum contact mode using chromium-on-quartz masks fabricated by Photronics Inc. (Dresden).

A typical microscope image of a straight DLSPP waveguide coupled to access Si-wire waveguides is depicted in Fig. 10. The cavity providing the necessary vertical offset between the two waveguides is clearly visible. Notice also the longitudinal metallic stripe gaps present in both waveguide transitions. Such gaps were observed in several fabricated structures.

B. Insertion Loss Measurements

Insertion loss measurements were performed on two separate sets of fabricated samples (chips) involving wire and rib

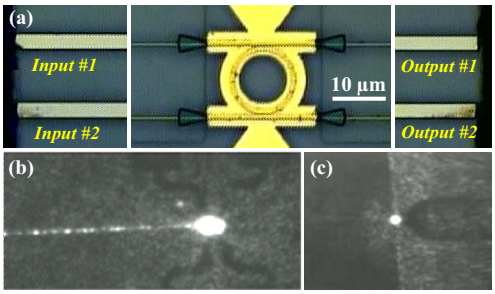

Fig. 11. Microscope images: (a) Add-drop WRR filter coupled to Si-wire waveguides. The sample termination regions featuring good end-facet quality are also depicted. (b) Scattering track of light coupled from a Si-wire waveguide (left-hand side) to the WRR filter. Electrodes for thermal tuning of the WRR filter are also visible. (c) Output chip edge showing scattered light and out-coupling tapered fiber.

SOI waveguides, respectively. In order to complete the measurement setup, samples were accessed with optical fibers. In the first case, wire SOI waveguides are coupled to polarization-maintaining (PM) tapered lensed fibers through inverted tapers. In the second, rib SOI waveguides are coupled to PM fibers through TM grating couplers.

1) Samples with Si-Wire Waveguides: We first focus on samples comprising wire waveguides. The nominal values of W_{Si} and H_{off} in these samples were 175 nm and 200 nm, respectively. Initial inspection of the chip containing several such samples showed good overall quality of the structures. Only some minor fabrication issues like misalignment of the plasmonic section and defective Si-waveguide end-facets were observed in certain cases. An example of a straight DLSPP waveguide properly aligned to in- and out-coupling Si-wire waveguides is depicted in Fig. 10. Unfortunately, none of these well-aligned straight DLSPP waveguide structures featured good end-facet quality as well. The latter is crucial for end-fire coupling to optical fibers required for transmission measurements. Thus, IL measurements were performed on add-drop WRR filters featuring good end-facet quality [Fig. 11(a)].

Insertion loss measurements were carried out using a tunable laser ($1480 - 1530$ nm) serving as the source and an optical spectrum analyzer serving as the detector. Polarization maintaining tapered lensed fibers with a 14-μm-long working distance and a 2.5-μm-wide spot diameter were utilized for end-fire coupling to the Si-wire waveguides. The polarization of in-coupling light was adjusted to be vertical to the sample surface. This was achieved by monitoring the output facet of the sample with the help of a far-field microscopic arrangement. Fig. 11(b) depicts the scattering trace of light coupled to a WRR filter from the left through a Si-wire waveguide. Scattered light in the output Si-wire waveguide is not clearly seen, because of the high propagation losses suffered in the DLSPP waveguide. However, a bright dot at the output facet is clearly visible [Fig. 11(c)], indicating that light does indeed reach the end-facet.

The fiber-to-fiber insertion loss for a reference Si-wire waveguide (without any DLSPP waveguide section) was first measured and found equal to approximately 45 dB for the wavelength range $1480 - 1520$ nm. For the WRR structure, fiber-to-fiber IL was approximately 50 dB for the same wavelength range, indicating an excess loss of 5 dB associated with the plasmonic section. We note that the spectral response of the WRR filter (through port) in this wavelength range was almost flat. This indicates that no coupling to the ring resonator was actually achieved, something also verified by the absence of any detectable signal at the drop port. The nominal gap values, i.e., the edge-to-edge separations between ring resonator and the two bus waveguides, for the WRR filter in question were 300 nm and 350 nm, respectively. However, the absence of coupling suggests that the actual gaps were probably larger. Since the absence of coupling implies absence of scattering loss as well, we infer that the excess loss of 5 dB comprises only propagation loss in the bus DLSPP waveguide and total interfacing losses. The length of the bus DLSPP waveguide in these WRR structures is 20 μm. Considering the propagation loss calculated for DLSPP waveguides (~ 0.1 dB/μm) and verified in our experiments [25], the propagation loss associated with the plasmonic section is ~ 2 dB. Hence, the coupling loss for the DLSPP-SOI interfaces is ~ 3 dB, in agreement with the theoretical findings of Section IV given the presence of longitudinal metallic stripe gaps in certain waveguide transitions.

2) Samples with Si-Rib Waveguides: We now turn to samples comprising rib SOI waveguides. Again, the nominal values of W_{Si} and H_{off} in fabricated samples were 175 nm and 200 nm, respectively. Since it was found rather difficult to ensure good edge quality necessary for achieving efficient coupling to access fibers (Section V-B1), these samples are equipped with TM grating couplers for fiber in- and out-coupling. The fabricated chip hosts, among others, a total number of nine straight DLSPP waveguides with varying lengths. Specifically, these include three 60-μm-, three 80-μm- and three 100-μm-long DLSPP waveguides. Each DLSPP waveguide is integrated into a 3-mm-long silicon waveguide terminated on both sides with TM grating couplers. The Si-rib waveguide propagation loss and the TM grating coupler efficiency were found to be 4.6 dB/cm and -12.5 dB, respectively, using a cut-back measurement approach on straight Si-rib waveguides included in the same chip.

Fig. 12 depicts the fiber-to-fiber insertion loss measurements for the aforementioned samples after subtracting the losses corresponding to the silicon part, namely, the Si-rib waveguide propagation loss and TM grating coupler efficiency. These loss values comprise DLSPP waveguide propagation loss and coupling losses associated with both input and output DLSPP-SOI interfaces. Least-squares linear fitting was performed on the measured data (solid line) resulting in a DLSPP waveguide propagation loss of 0.1 dB/μm (Fig. 12). Given that this value is well established in both theory and experiment, we can subtract the loss associated with propagation along the DLSPP waveguide in each case according to the respective length and end up with pure interfacing losses. Specifically, the coupling loss per interface varies from -2 to -4.5 dB, with a mean value of -3.2 dB and a standard deviation of 0.85 dB. This result is in fair agreement with the 2.85-dB insertion loss calculated for the 0.5-μm-gap variant of the DLSPP to Si-rib waveguide transition with optimal geometrical parameter

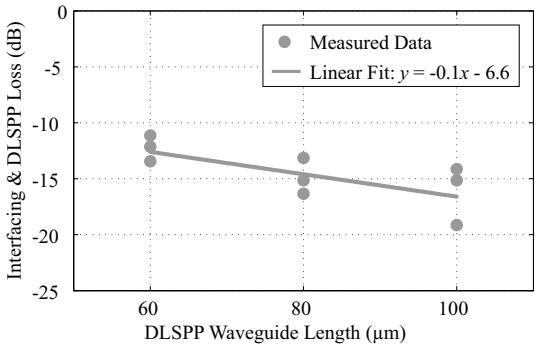

Fig. 12. Insertion loss measurements for the nine DLSPP waveguide structures of varying length. Plotted values include total interfacing losses and DLSPP waveguide propagation losses (The Si-rib waveguide propagation loss and TM grating coupler efficiency have been subtracted.). Linear fitting indicates a DLSPP waveguide propagation loss of 0.1 dB/μm. Interfacing losses range from -2 to -4.5 dB per interface depending on the sample in question.

settings in Section IV-B. The high dispersion of the measurements is attributed to lateral misalignment between waveguides and the actual stripe-gap length values in different samples.

VI. Summary and Conclusion

To summarize, we have presented a comprehensive theoretical analysis of end-fire coupling between DLSPP and compact SOI waveguides. Both rib and wire variants of the SOI waveguide have been examined. In each case, the interface geometrical parameters leading to optimum performance have been identified, and the fabrication tolerances about these optimum parameter values quantified. The highest coupling efficiency has been attained with the wire variant and equals 85 % (IL $= -0.7$ dB). Furthermore, the effect of a longitudinal metallic stripe gap on coupling efficiency has been assessed since such gaps have been observed in fabricated samples.

In order to verify the theoretical findings, we have conducted insertion loss measurements on two separate sets of fabricated samples comprising wire and rib waveguides, respectively. In the first case, coupling loss has been estimated to -1.5 dB per interface, whereas in the second, coupling losses ranging between -2 and -4.5 dB per interface have been reported. Both results are consistent with the theoretically anticipated values.

In conclusion, the efficient transition between planar plasmonic and silicon photonic waveguides reported here and elsewhere [15]–[20], should enable the hybridization of the two most prominent technologies for nanophotonic circuits, namely, plasmonics and silicon photonics. This paves the way for hybrid silicon-plasmonic circuits, such as the one proposed in [30], benefiting from the distinct advantages of each platform.

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